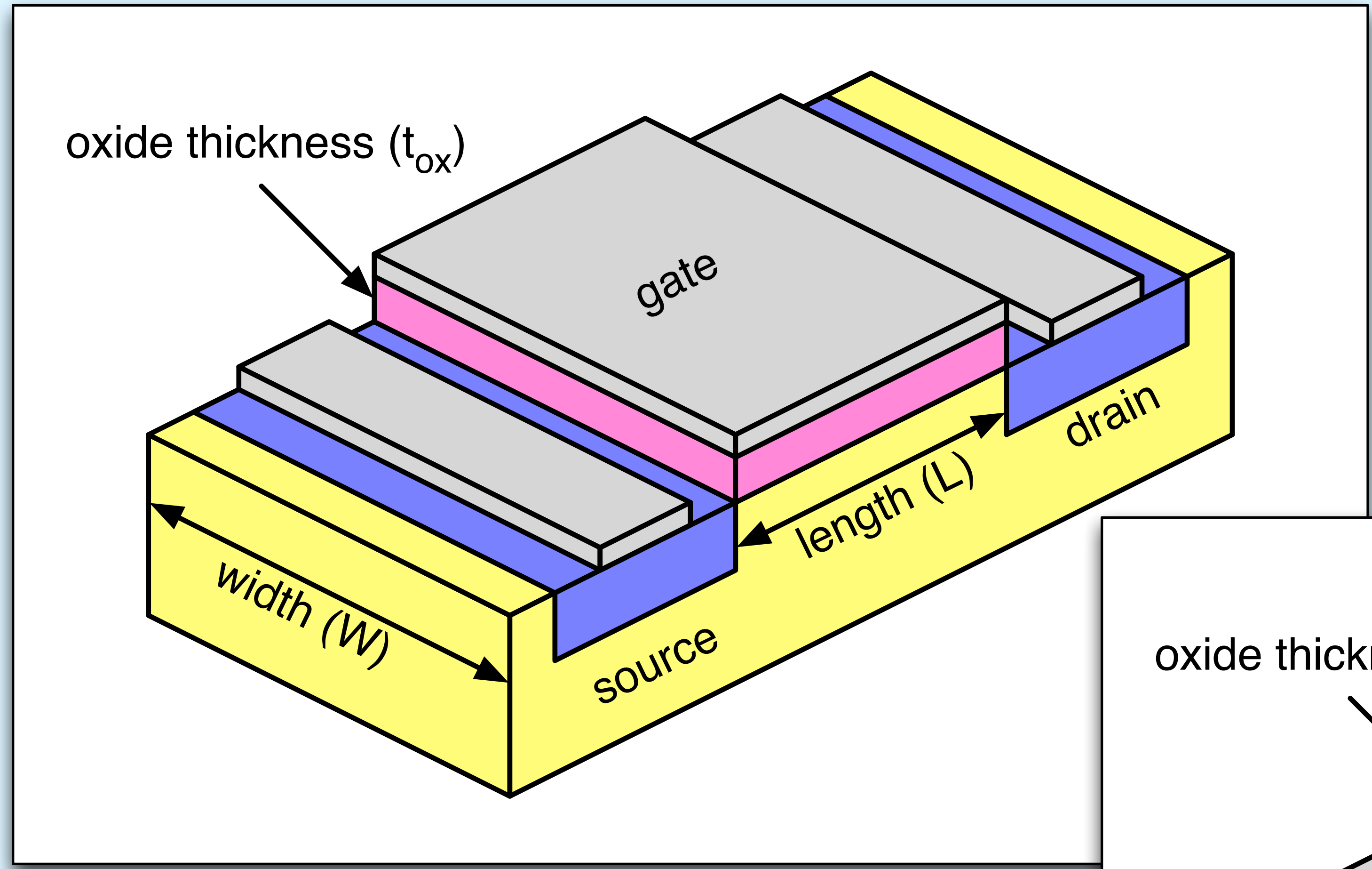
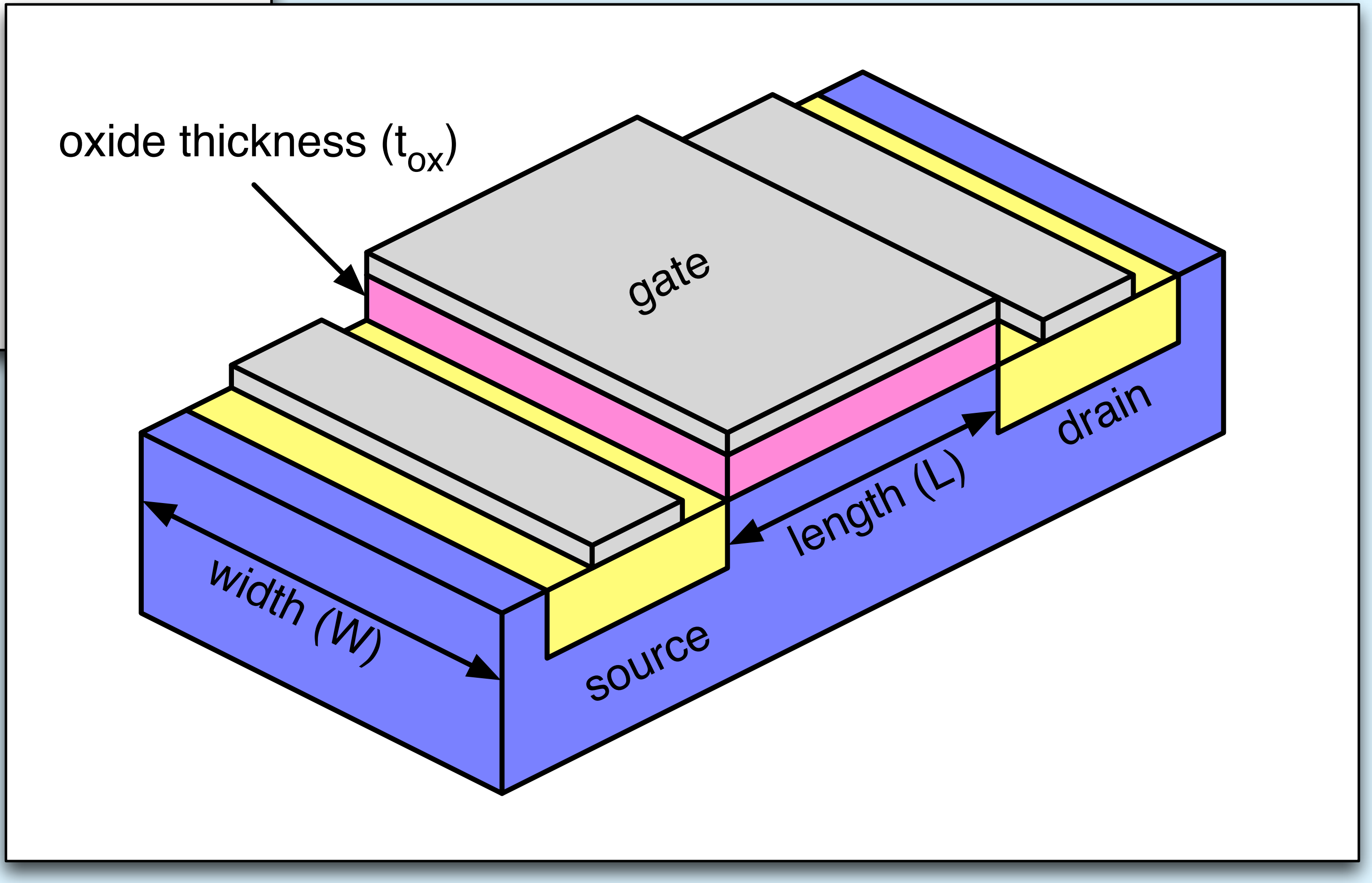


NMOS



PMOS

NMOS + PMOS = CMOS

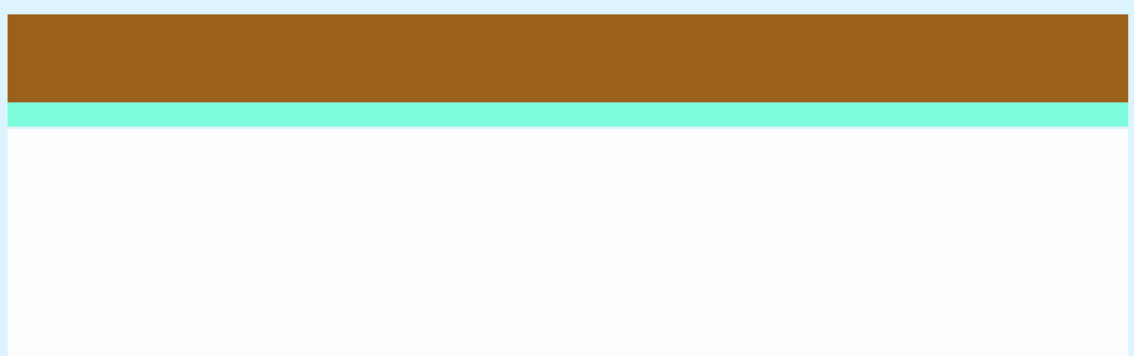
gate length

oxide thickness

Overview of a modern CMOS process

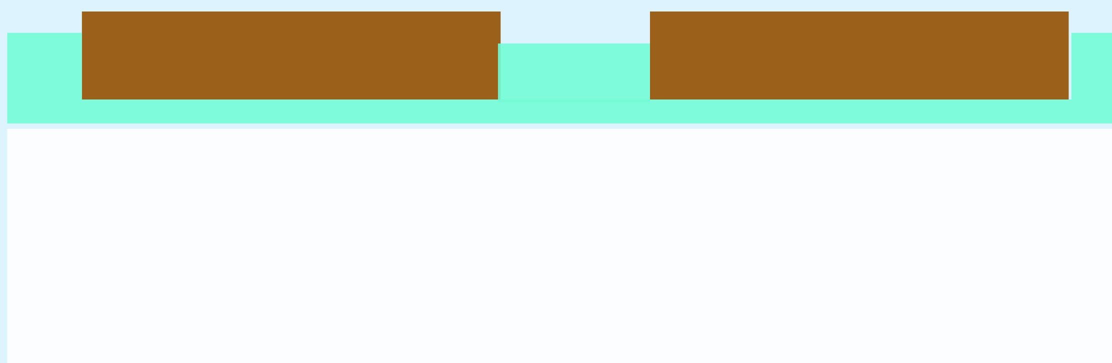
1. starting silicon wafer (low-doped)

2. grow a thin “pad” oxide



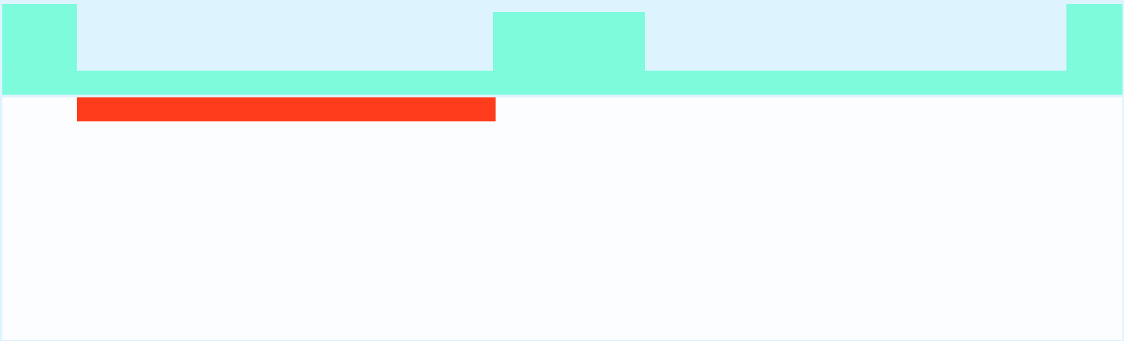
3. deposit silicon nitride

4. pattern and etch SiN

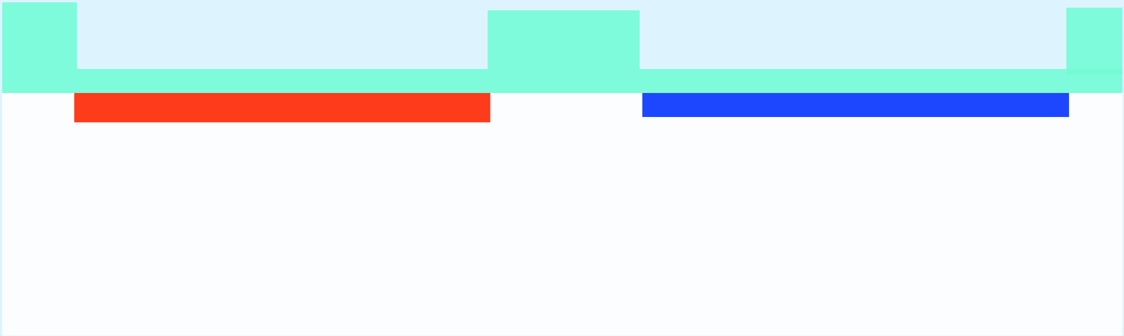


5. grow LOCOS oxide (device isolation)

6. strip nitride & thin oxide, 7. grow thin screening oxide

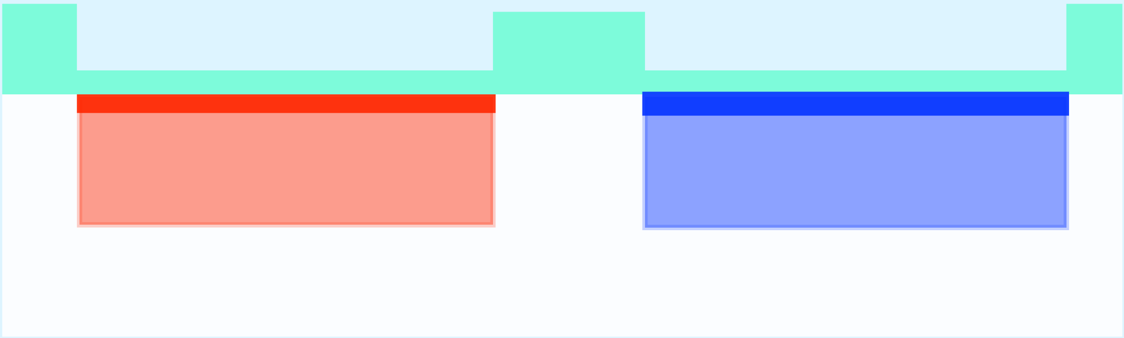


8. lithography, ion implant donors for n-well

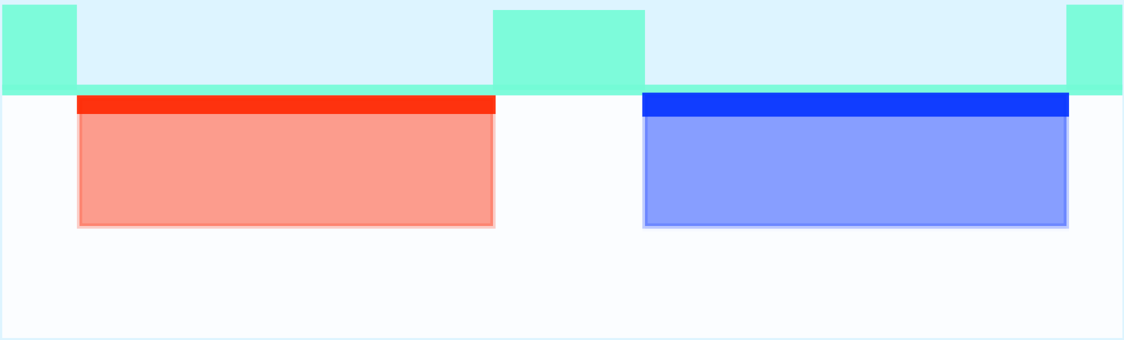


9. lithography, ion implant acceptors for p-well

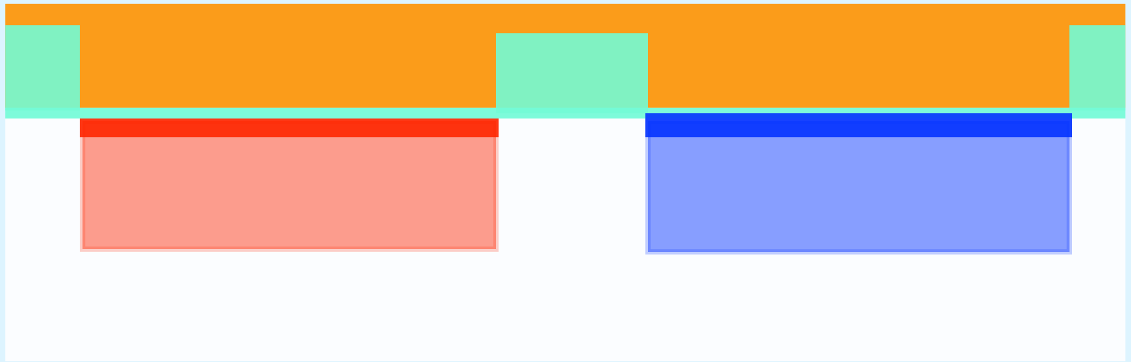
10. diffusion to drive dopant deeper in the wells



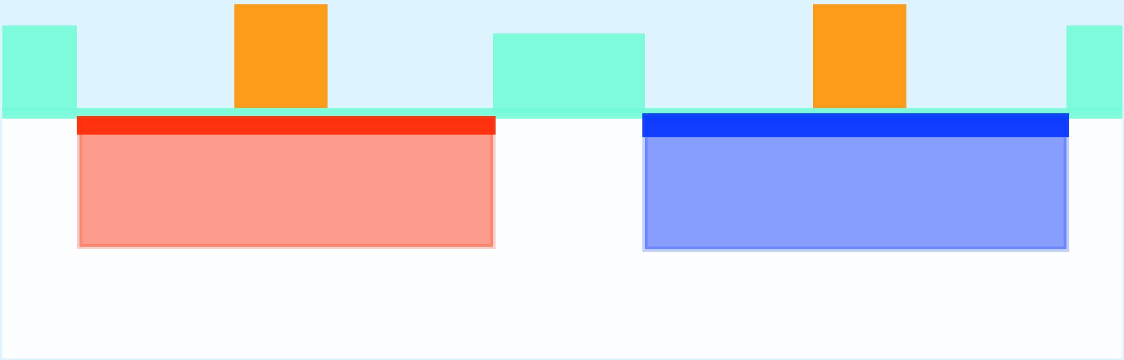
11. Lithography and threshold adjust implant in n-well
12. Lithography and threshold adjust implant in p-well



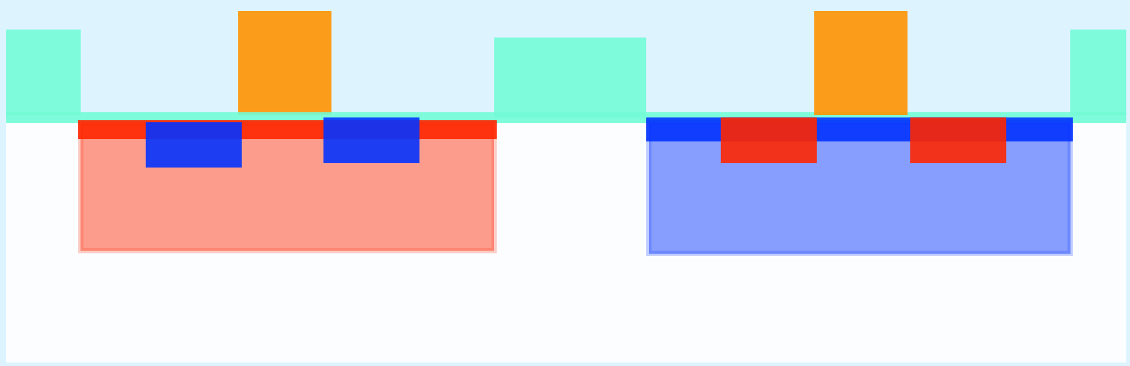
13. Lithography and strip oxide from device regions
14. grow thin gate oxide (critical step)



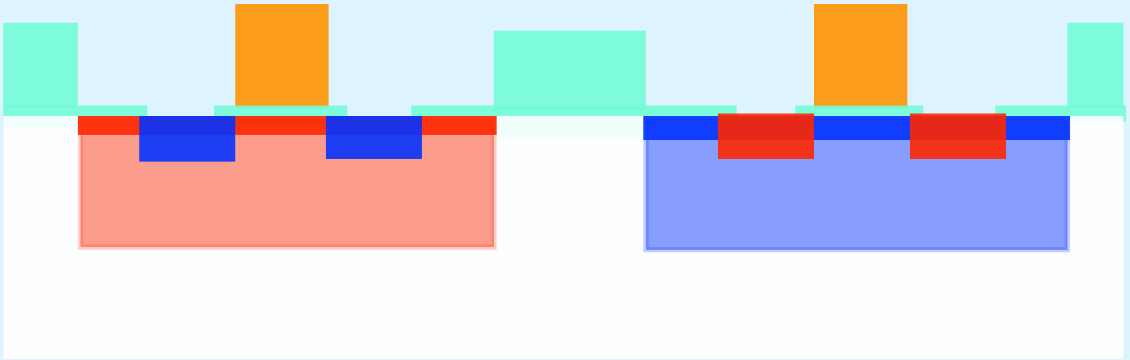
15. deposit polysilicon over entire wafer using CVD
16. dope it heavily by diffusion or ion implantation



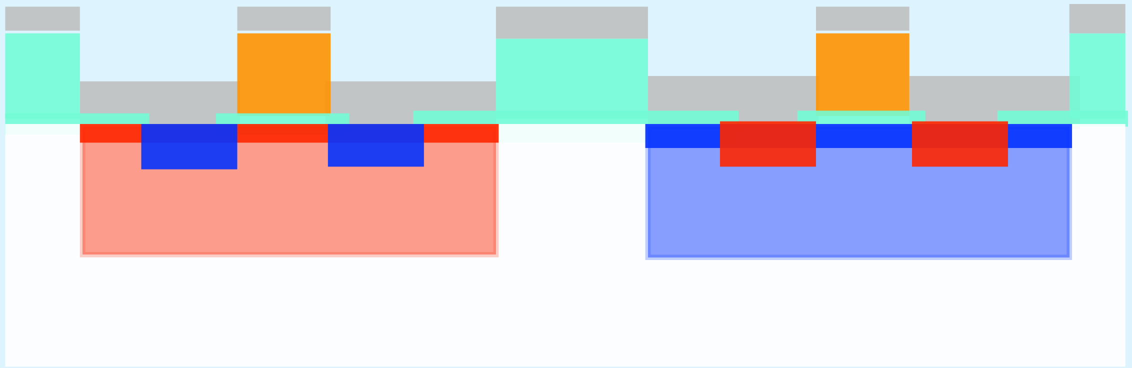
17. lithography and etch to form gates



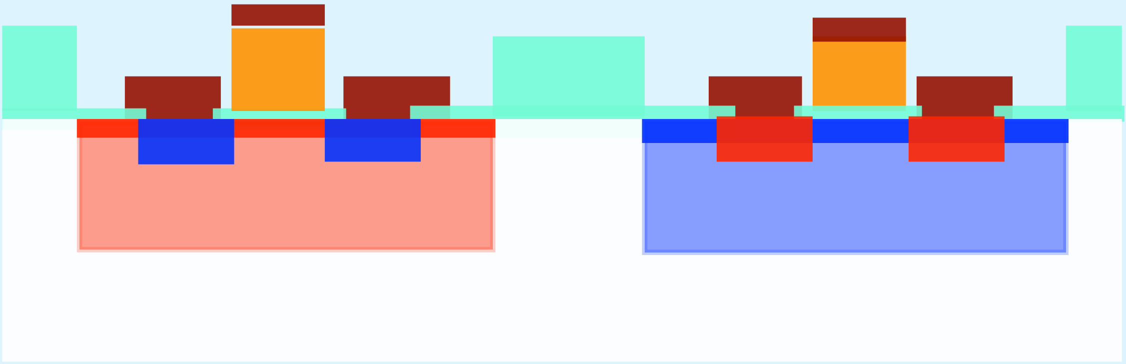
18. lithography and implant for pmos source/drain
19. lithography and implant for nmos source/drain



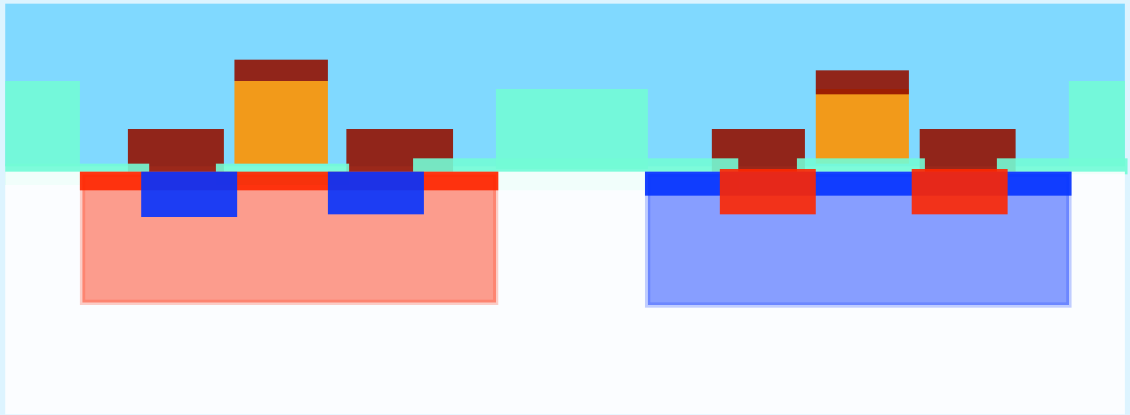
20. lithography and etch for device contacts



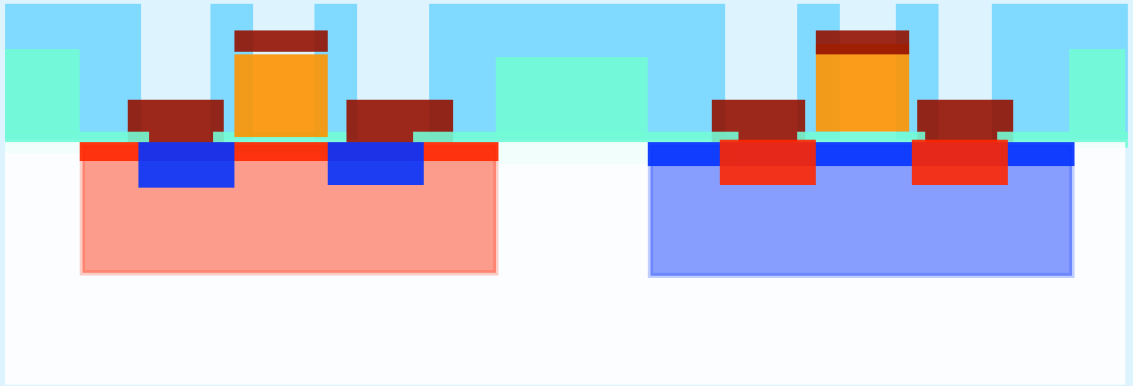
21. deposit titanium



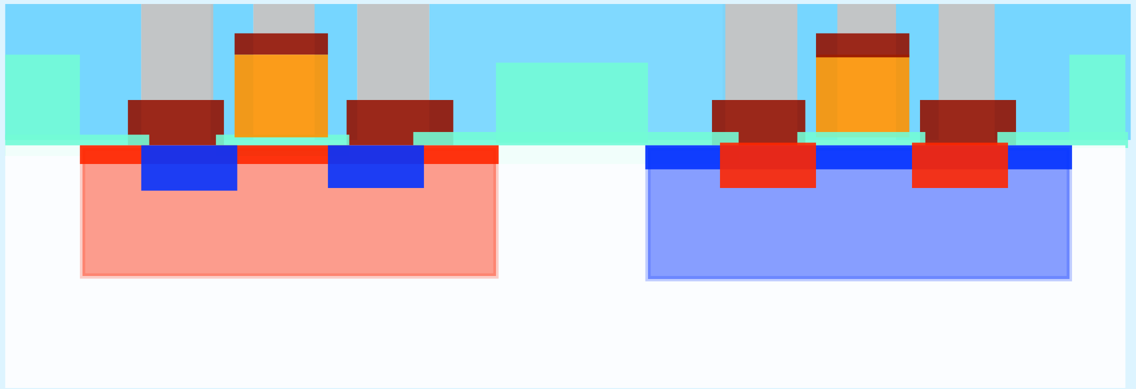
22. Lithography and etch contacts
23. Anneal to form TiSi/TiN composite contacts



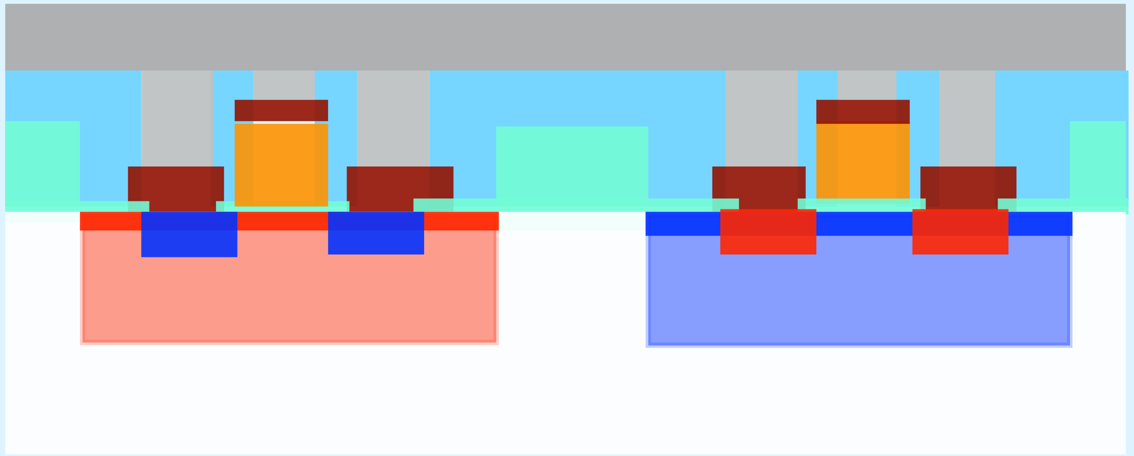
24. deposit oxide by CVD
25. planarize by CMP (critical step!)



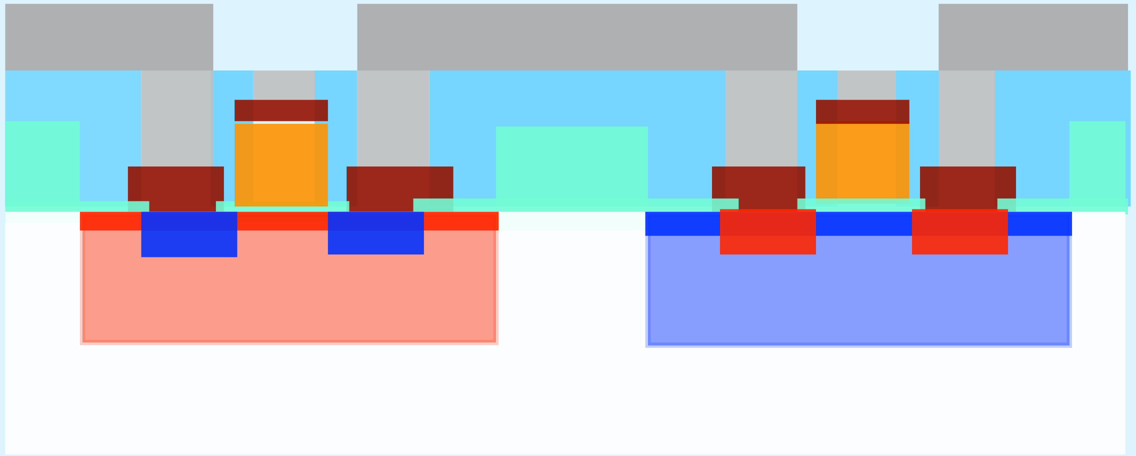
26. lithography and etch to form contact vias



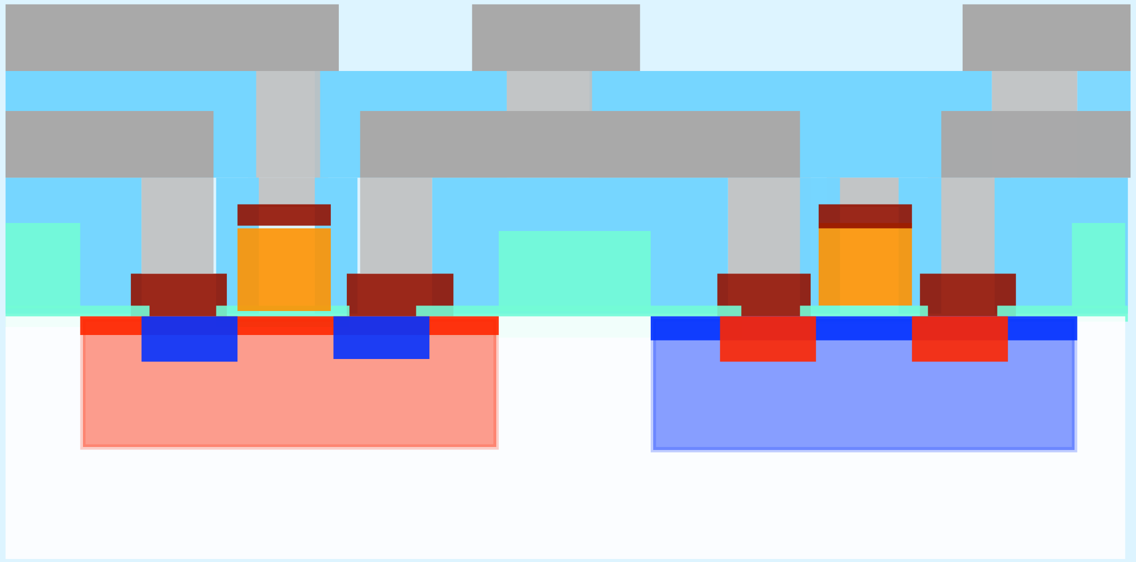
27. Use selective CVD to fill vias with tungsten “plugs”



28. Deposit interconnect metal



29. lithography and etch to form interconnect traces



30+. Repeat to form subsequent interconnect layers

The various steps

- oxidation
- sub-micron lithography
- ion implantation and diffusion
- CVD to grown nitride and oxide layers
- plasma etching
- different metals (and means to deposit those)
- chemical-mechanical polishing
- multi-level interconnects