Copper interconnects

Copper advantages:

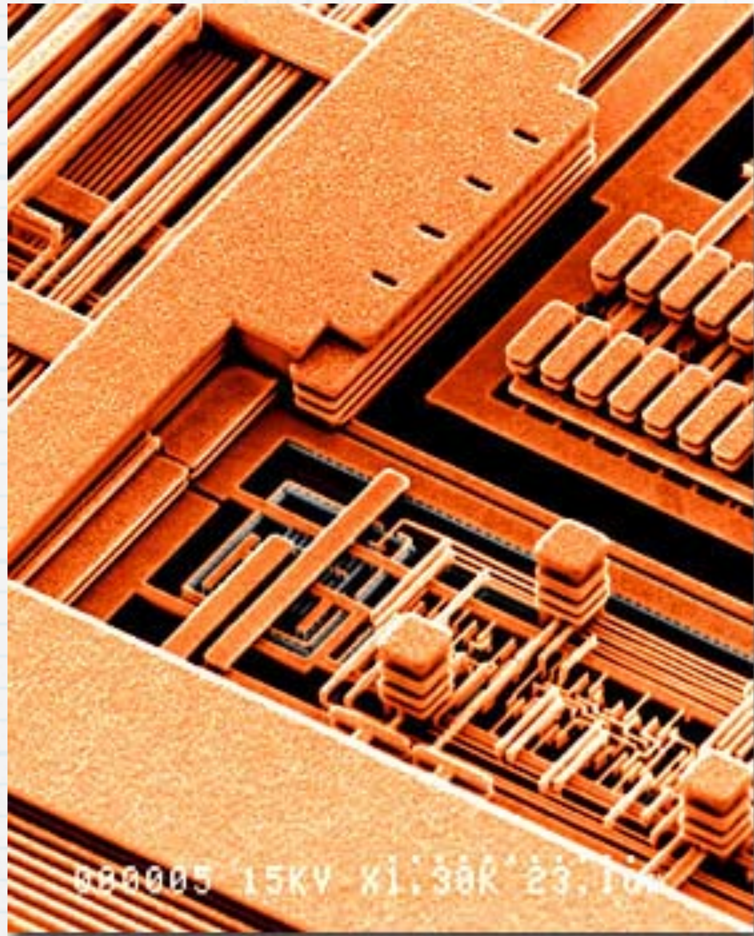
1. slightly better conductivity
2. much less susceptibility to *electromigration*

Copper disadvantages:

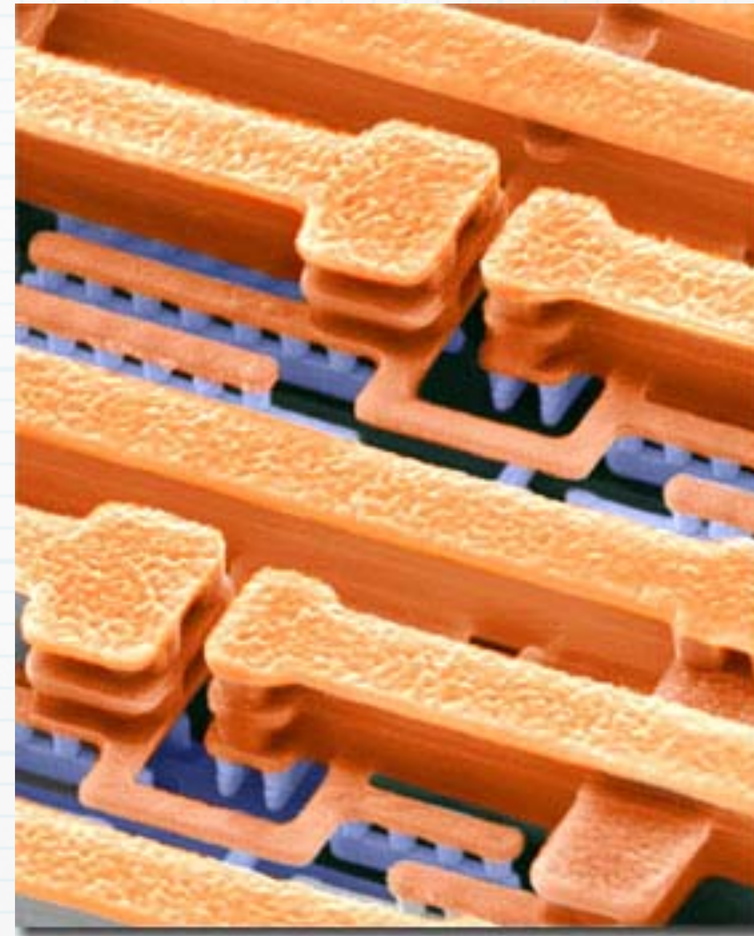
1. Creates deep level defects in silicon (i.e. *poisonous* for electronic devices)
2. Difficult (even impossible) to etch by plasma methods

Any method to utilize the advantages of copper must:

1. Keep the copper away from the silicon. Cannot be used for ohmic contacts, only for interconnects.
2. Patterns must be formed in a way that doesn't require directly etching the copper.



SEM view of Copper Interconnect
(IBM Microelectronics)



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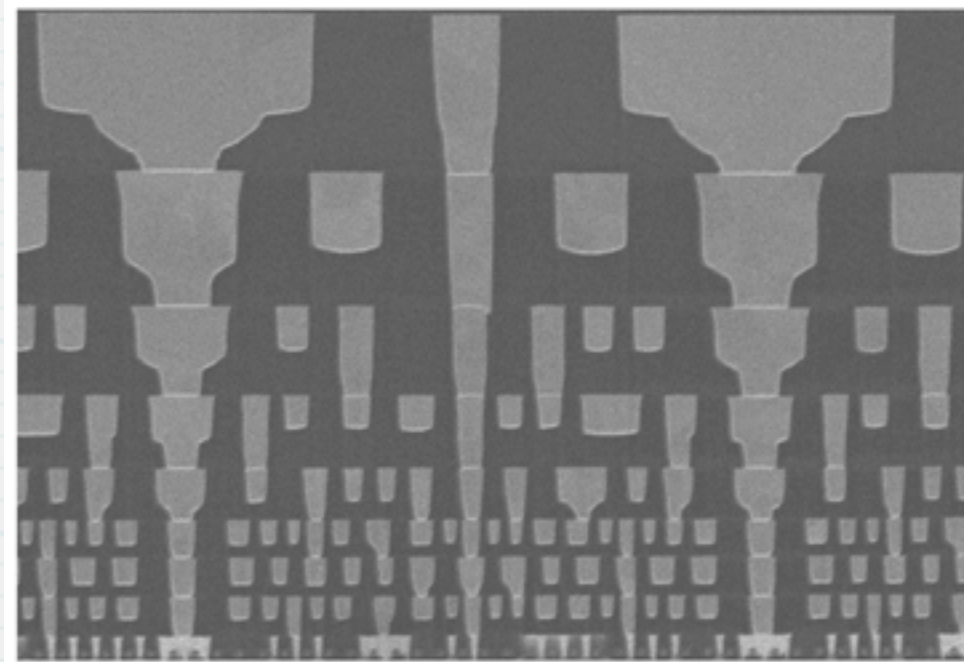
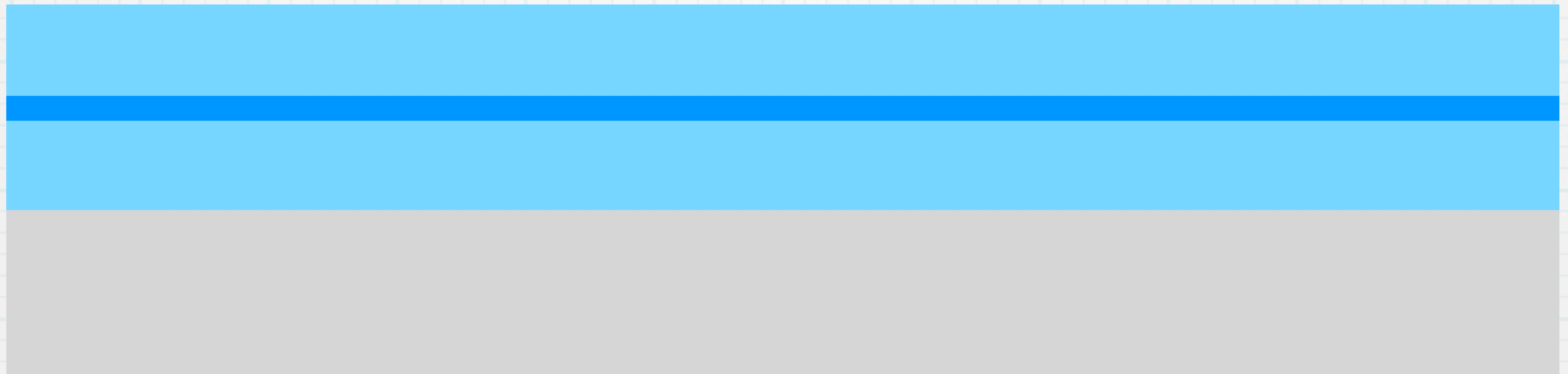


Damascene process

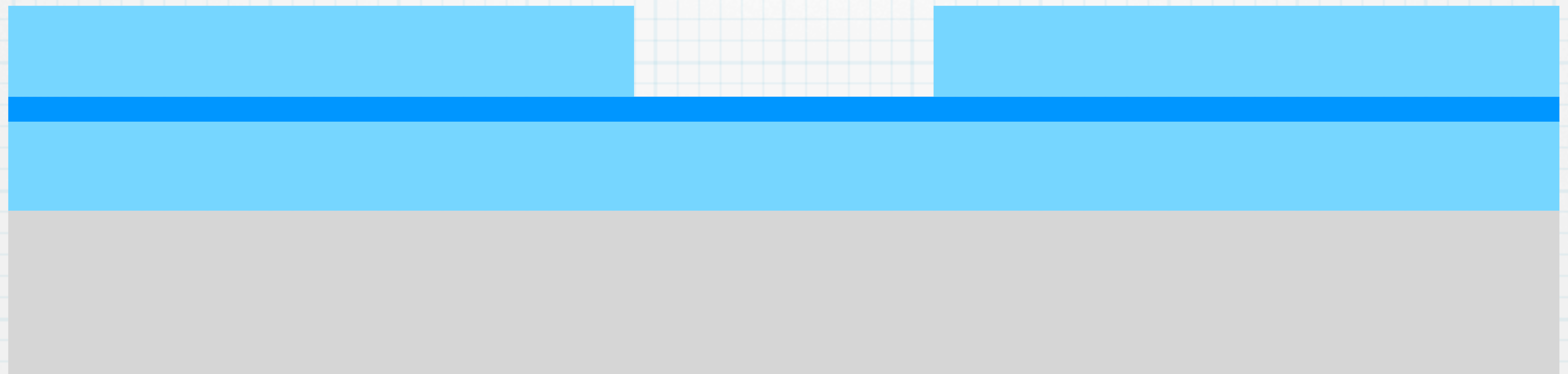
In middle ages, metal-smiths in Damascus developed processes for making intricately patterned, highly polished steel that was used extensively for making swords and knives. The steel was significantly better than anything else at the time. (Cutting edge technology!)

Technique for Damascus steel has been lost. Modern analysis of the metal shows that carbon nanotubes (!) are present and may have played a role in determining the properties.

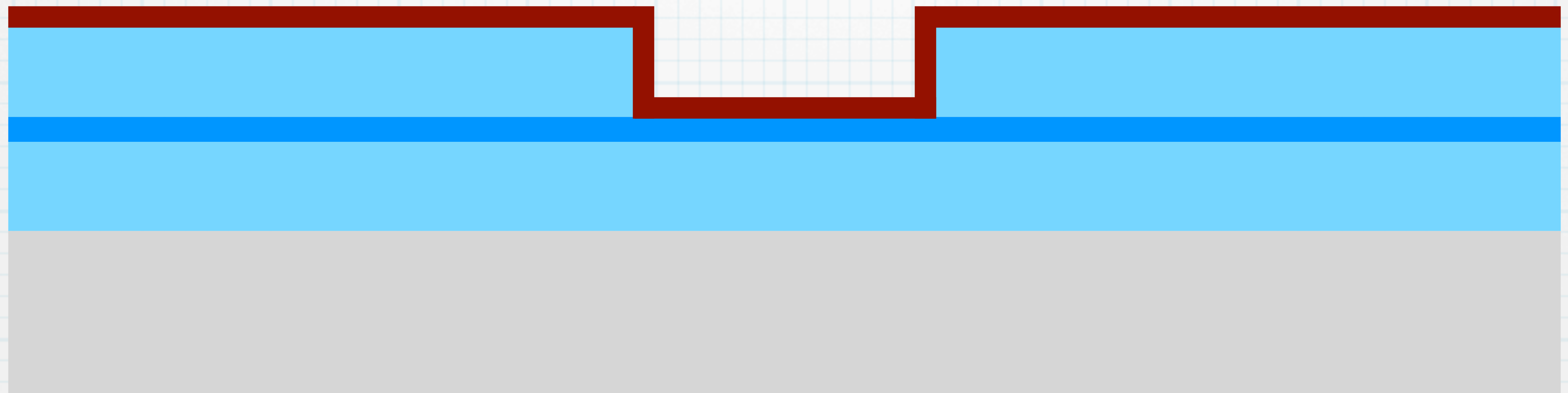
Damascene process



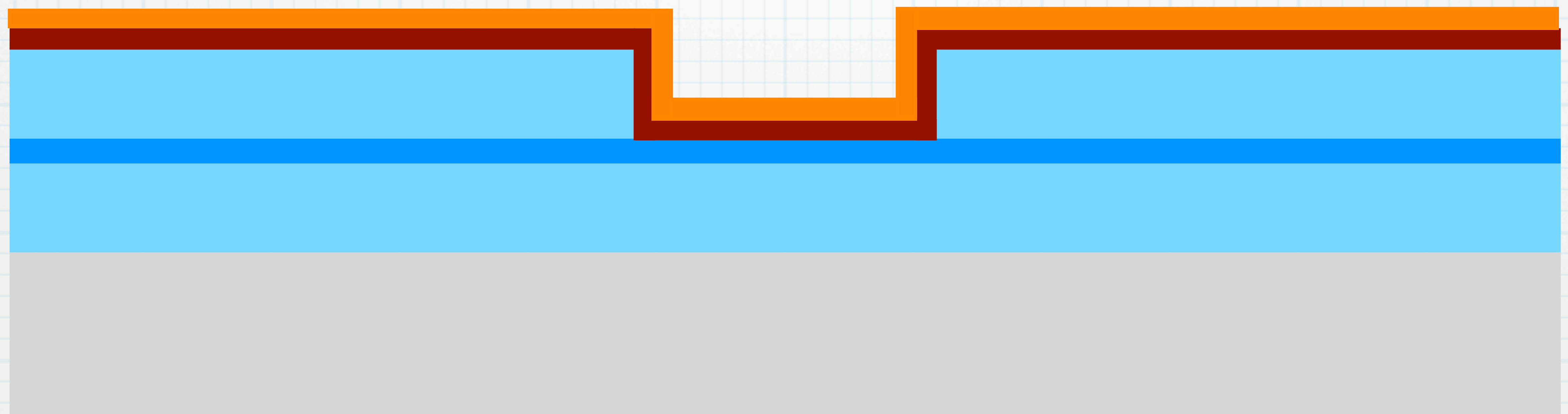
1. Using plasma-enhanced CVD, grow a stacked structure of silicon dioxide and silicon nitride. The silicon nitride will serve as an etch-stop layer.



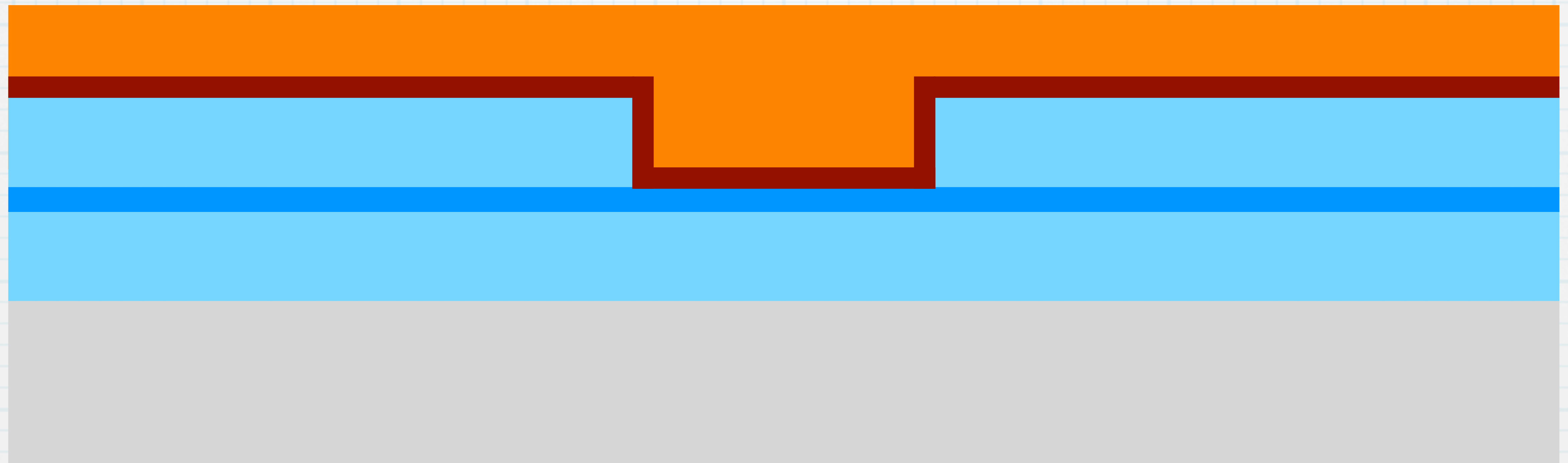
2. Using lithography and plasma etching, etch a trench in the upper oxide layer. The etch stops at the silicon nitride layer.



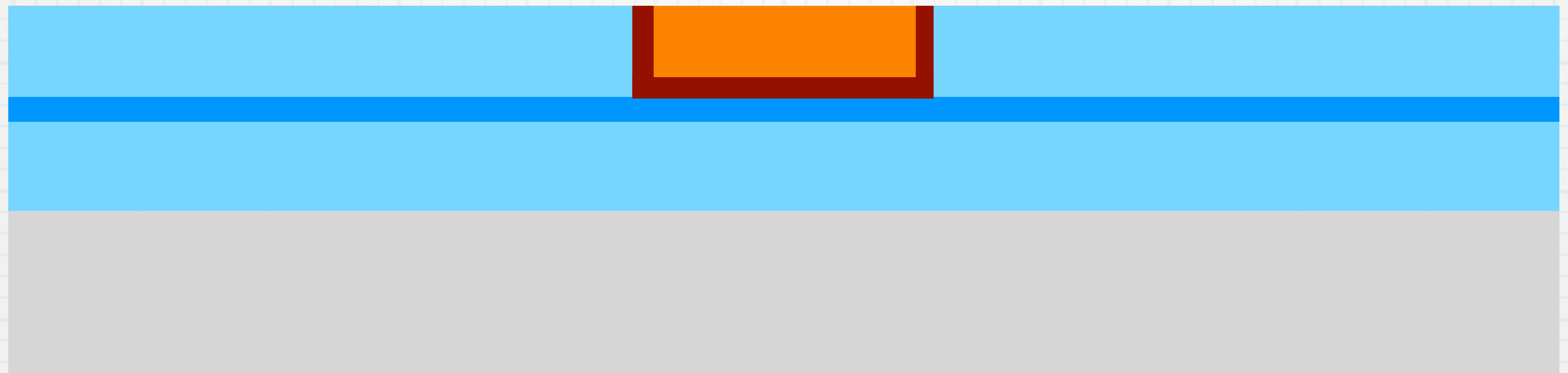
3. Using sputtering, deposit a thin layer of *titanium nitride* – TiN – over the top surface. The thickness is 10 nm or less. TiN is a very dense ceramic and prevents Cu atoms from diffusing through. Thus, its primary purpose is to form a diffusion barrier to keep the copper from the silicon. However, it also fairly conductive (≈ 50 μΩ·cm) and so current can flow through.



4. A thin layer of copper (≈ 10 nm) is sputtered over the TiN. The thin copper serves as a *seed layer* for the next step...



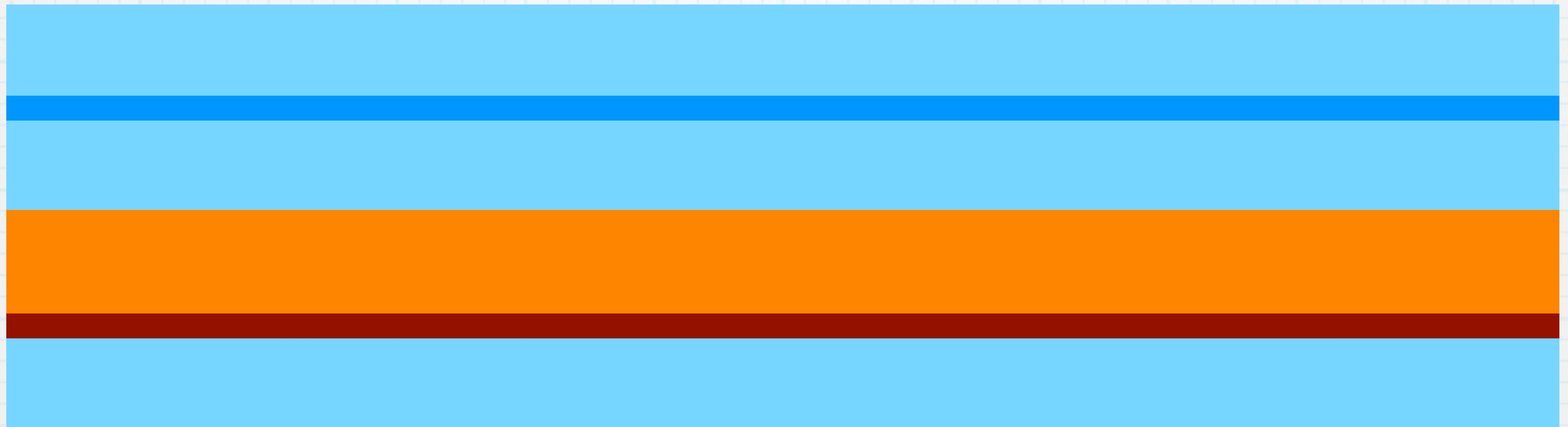
5. A thick layer of copper is deposited by electrolysis, using the seed layer as a starting point. This is essentially the same process that you may have used in grade school science class to deposit copper onto a spoon.



6. Finally chemical-mechanical planarization is used to grind away the upper portion of the copper, leaving only the portion in the trench. The top surface is flattened and ready for the next metalization step.

Dual damascene process

Inter-level vias can also be incorporated with a slight modification.



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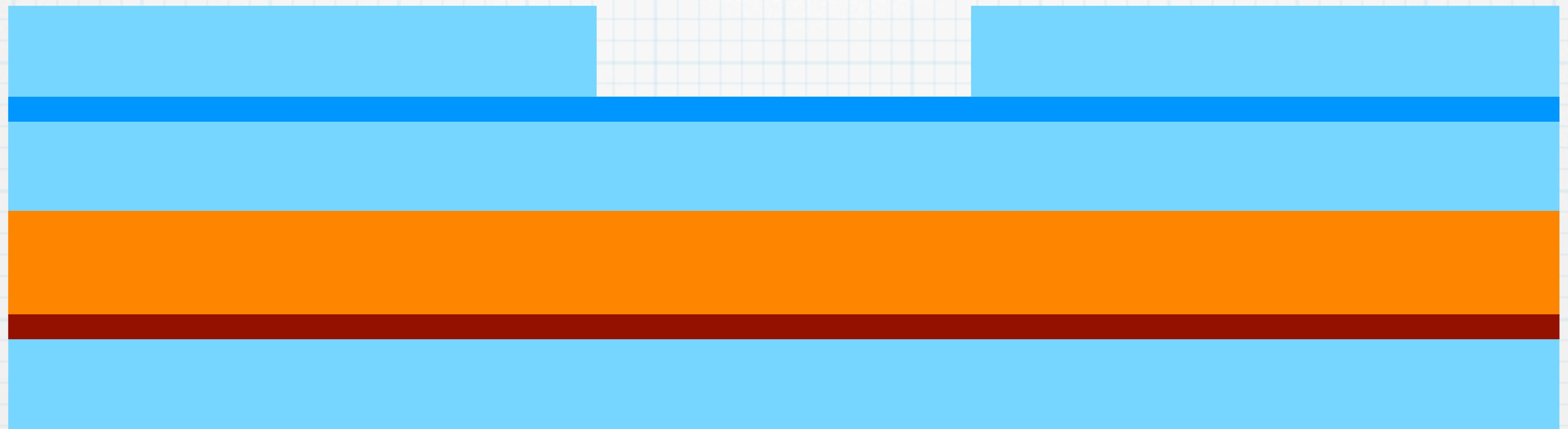
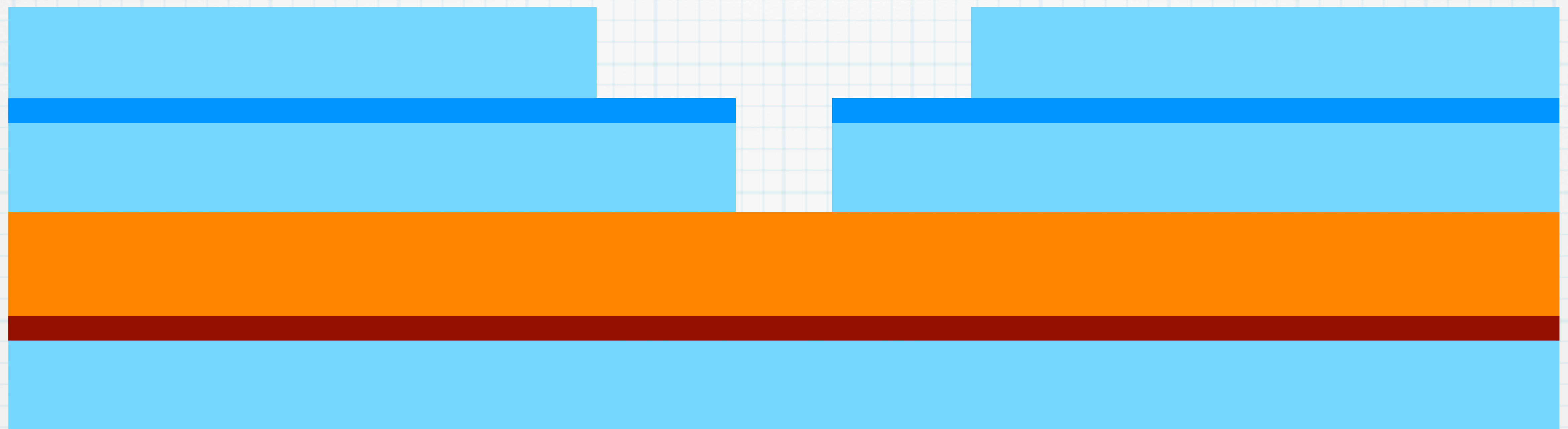
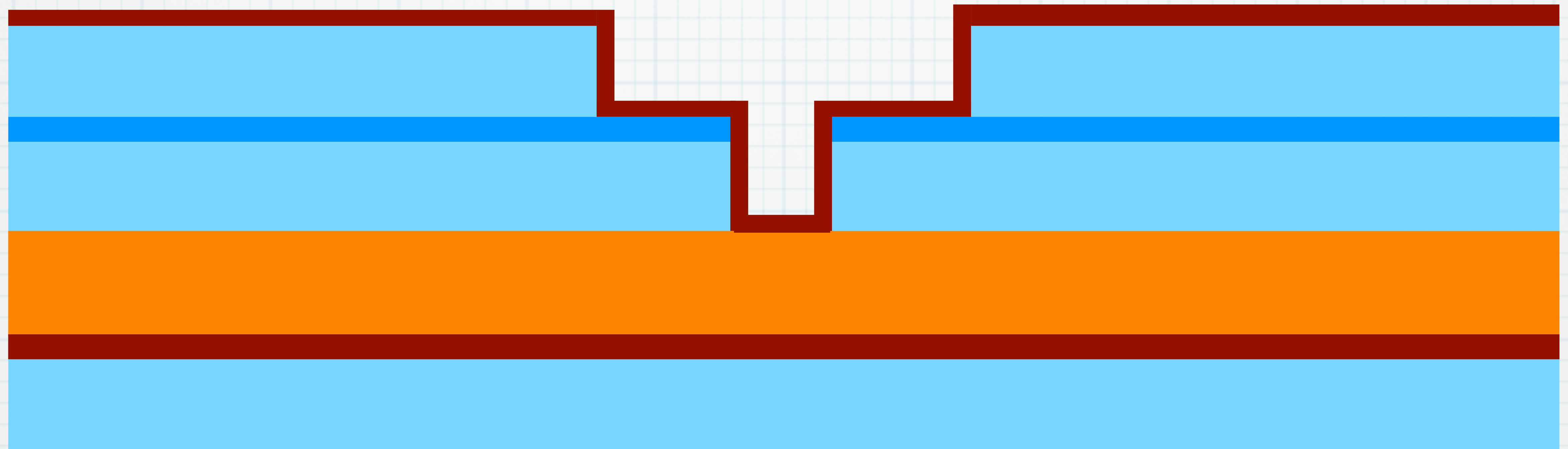


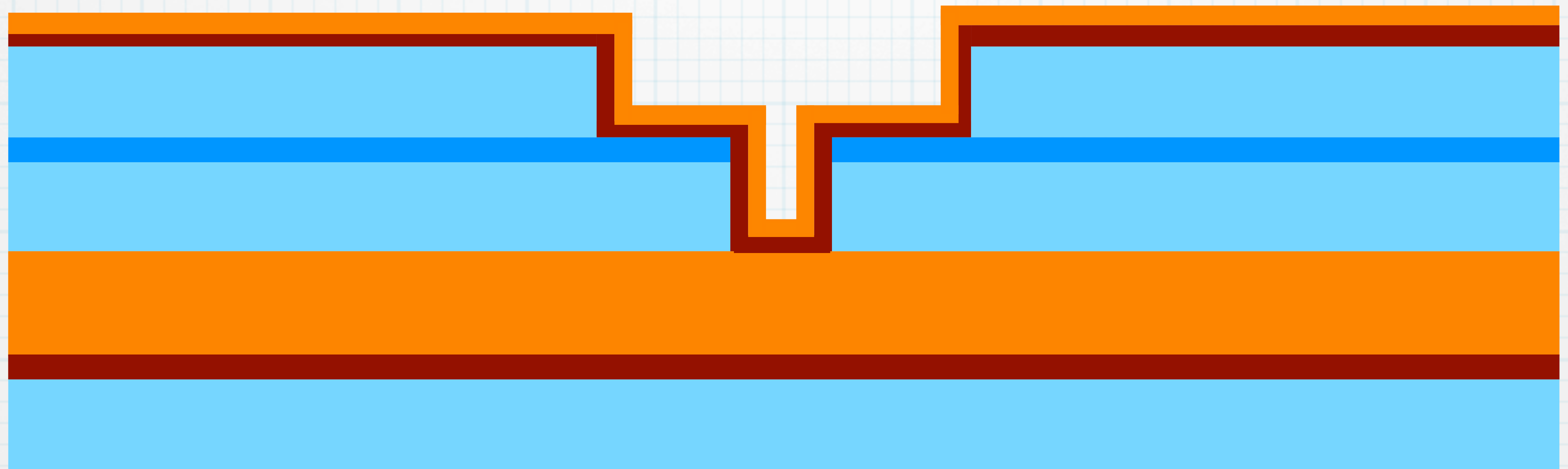
2. Using lithography and plasma etching, etch a trench in the upper oxide layer. The etch stops at the silicon nitride layer.



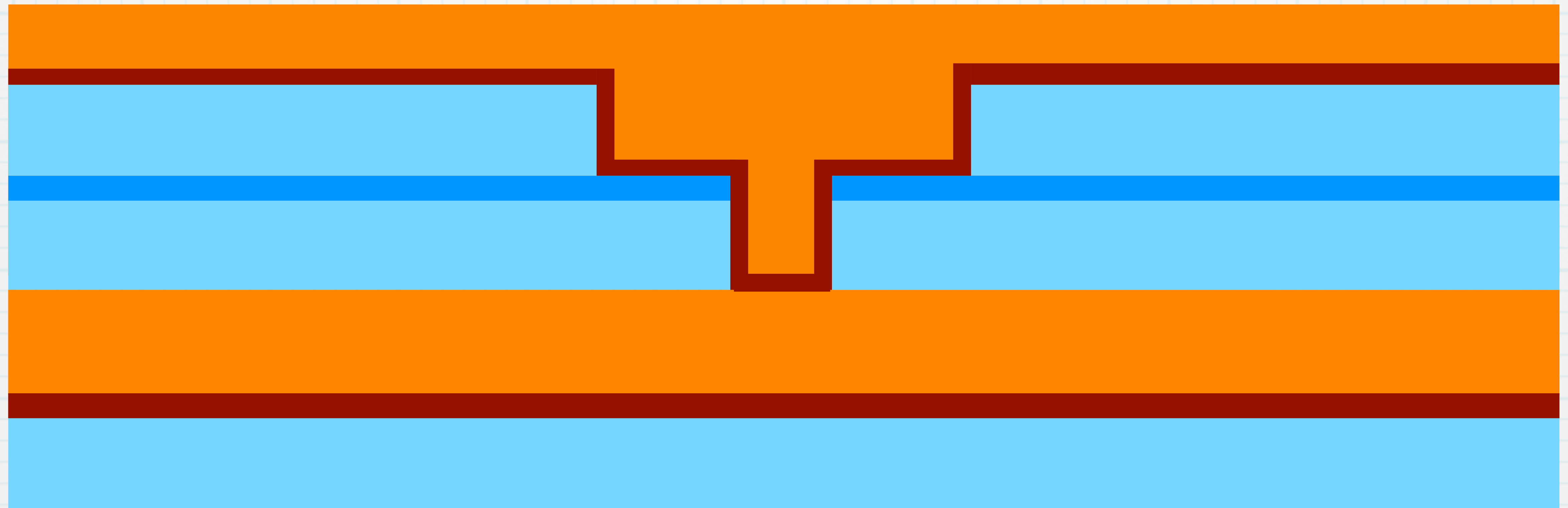
3. Using lithography and plasma etching a second time, etch a via in the lower oxide layer. The etch stops at the underlying copper interconnect.



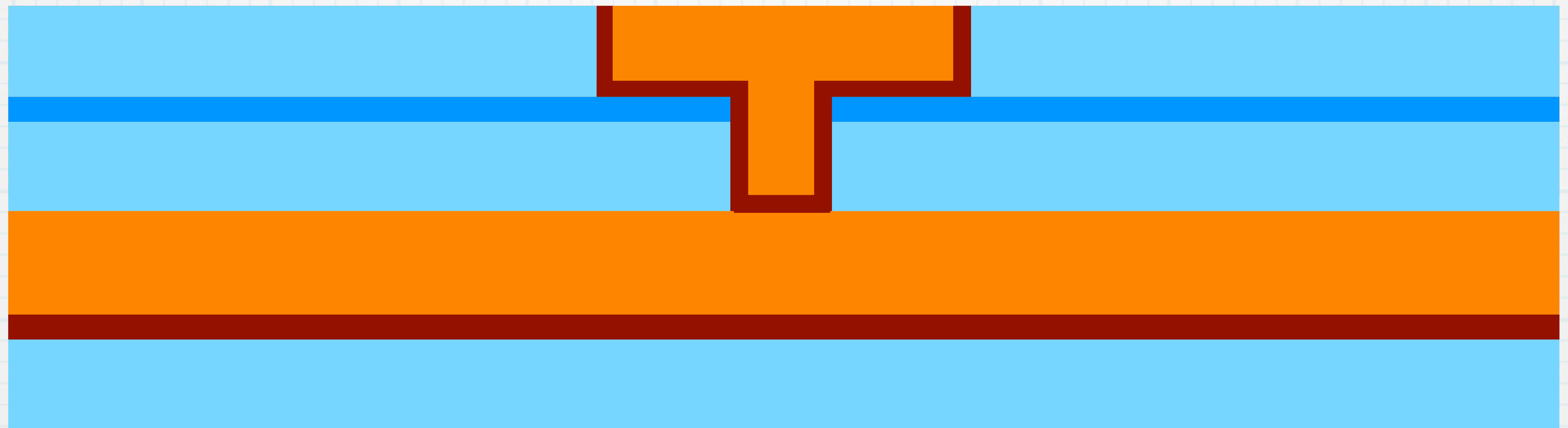
4. Using sputtering, deposit the thin TiN diffusion barrier.



5. Sputter on the thin seed layer of copper.



6. Deposit a thick layer of copper using electrolysis.



7. Use CMP to remove the excess copper, leaving behind the upper level interconnect and the via between the upper and lower connects.

With the dual damascene process, a separate via technology is not necessary. It is apparent why the TiN barrier material must also be conductive.