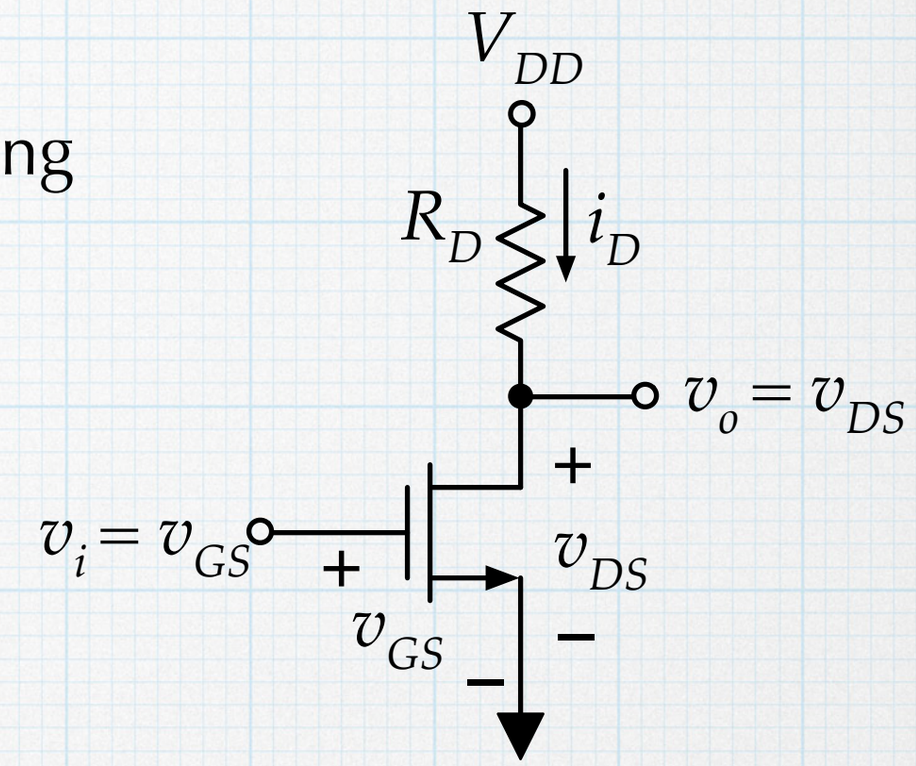
resistively-loaded NMOS inverter

We have seen the circuit at right while practicing our NMOS skills. Now we note that it is an implementation of a simple inverter.



The inverter input voltage is v_{GS} and the output is v_{DS}.

$$v_o = v_{DS} = V_{DD} - i_D R_D.$$

Since the drain current depends on the gate voltage (= v_i), it is easy to relate the output to the input.

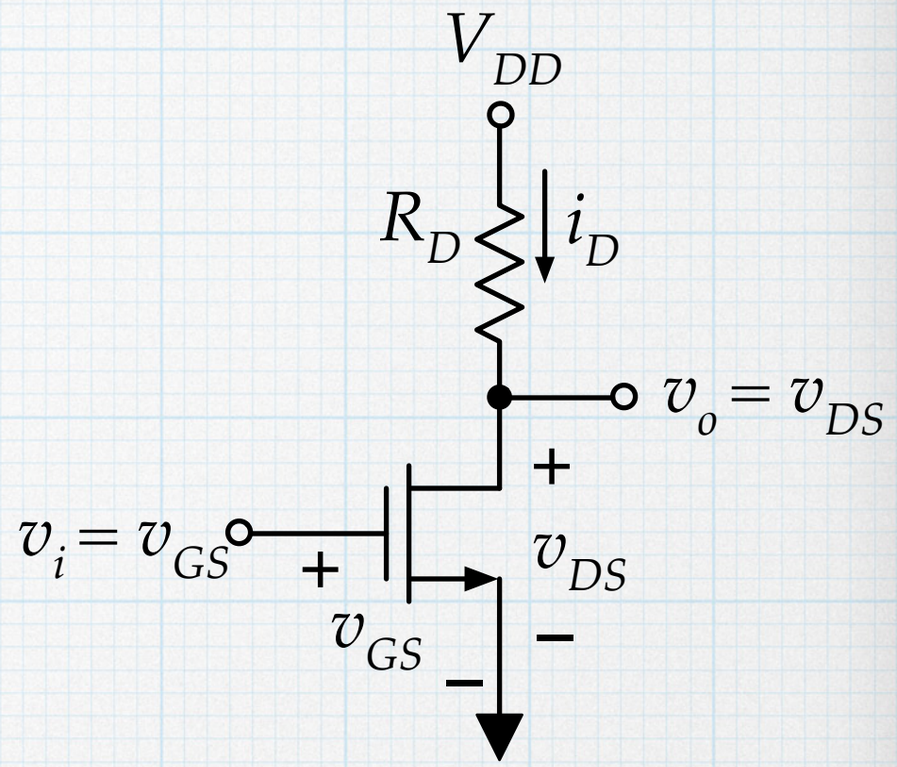
Determining the complete voltage transfer characteristic involves finding v_o as a function of v_i for all possible operating modes of the NMOS (off, saturation, ohmic) and putting the pieces together into a single characteristic.

In principle, the output voltage can range from 0 to V_{DD}. This also defines the range of the input voltage.

load-line diagram

A helpful visual guide in finding the voltage transfer characteristic is the *load-line diagram*.

Since the currents must be equal, if we plot the i-v curves for the resistor (the load) and the transistor on the same set of axes (i_D vs v_{DS}), the point where the curves intersect gives the particular operating point ($i_R = i_D$ and v_{DS}).

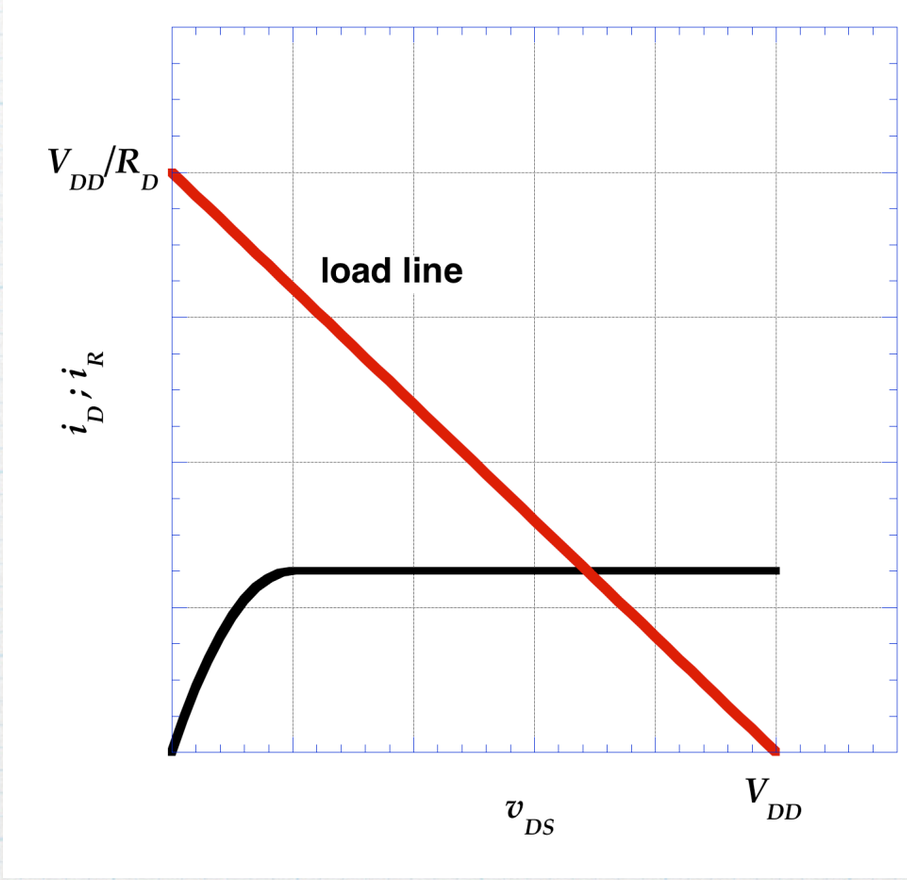


The resistor determines the load-line:

$$i_R = \frac{v_R}{R_D} = \frac{V_{DD} - v_{DS}}{R_D}$$

In this case, the load line is static – it is independent of what is going on with the transistor.

The transistor curve depends on the particular value of input voltage (v_{GS}).

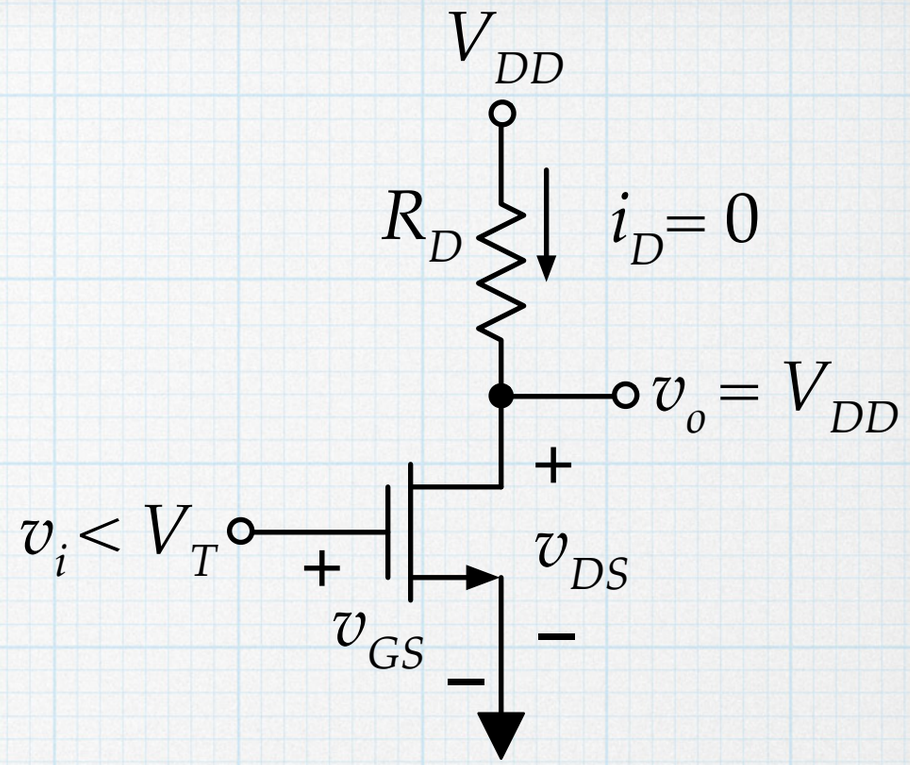


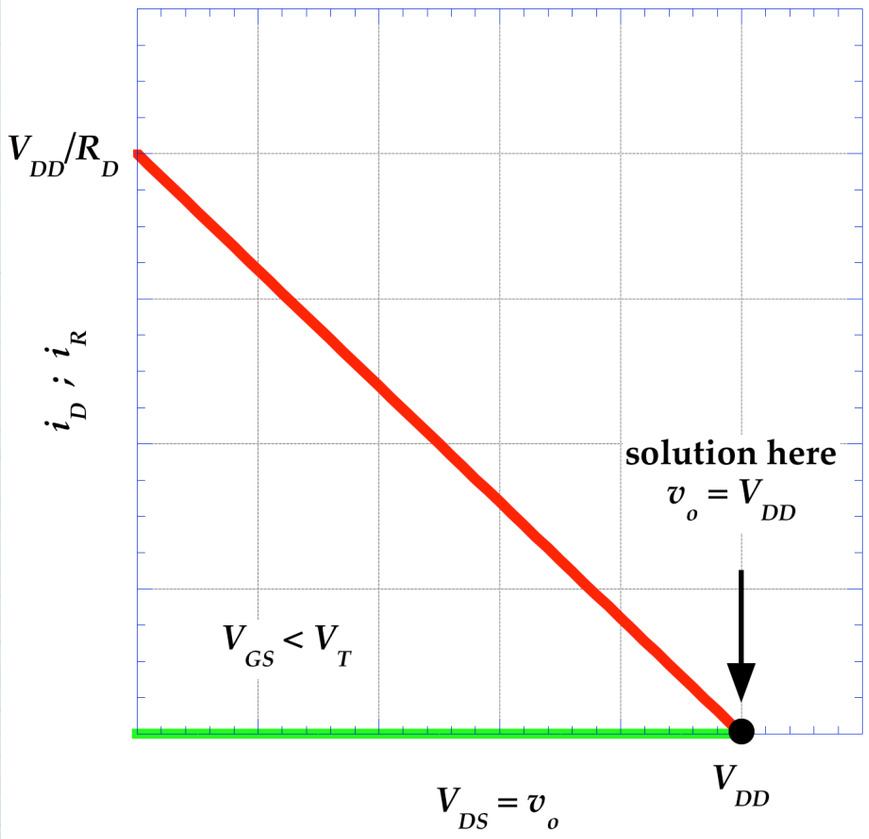
NMOS off

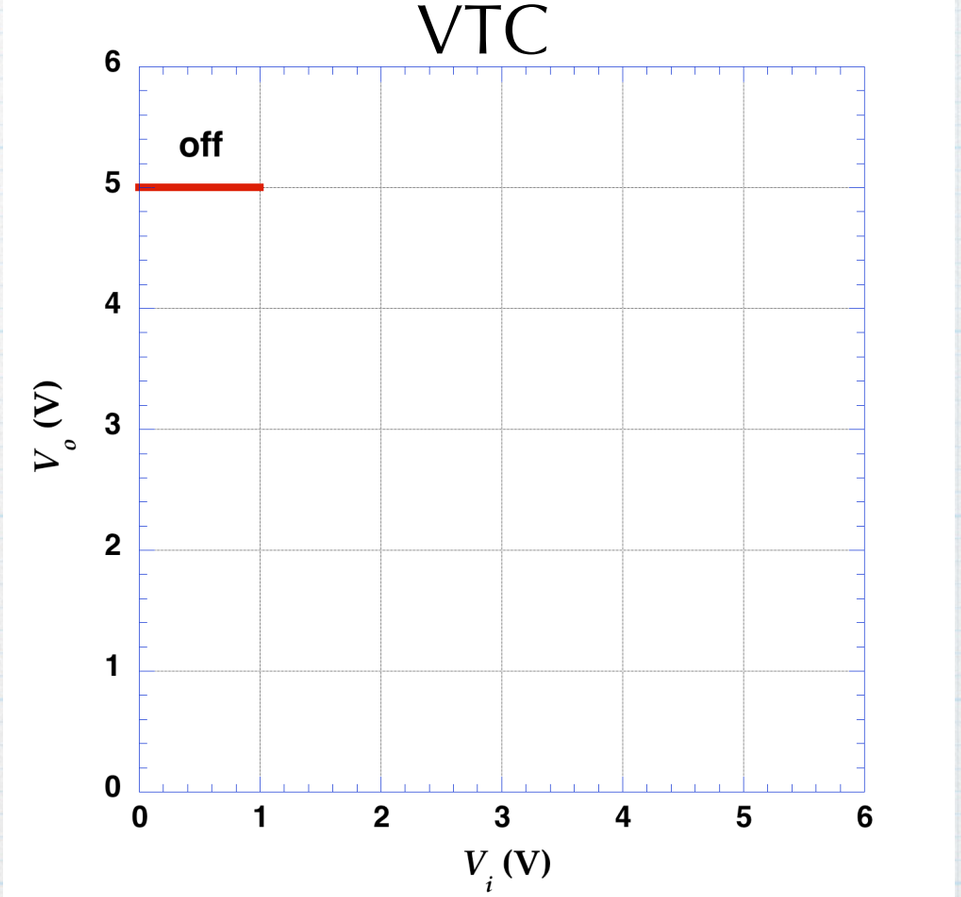
If $v_i < V_T$ for the NMOS, the transistor will be off and $i_D = 0$.

With the NMOS off, $v_o = V_{DD} - i_D R_D = V_{DD}$.

A load-line diagram probably isn't necessary in this case, but it confirms what we know intuitively.

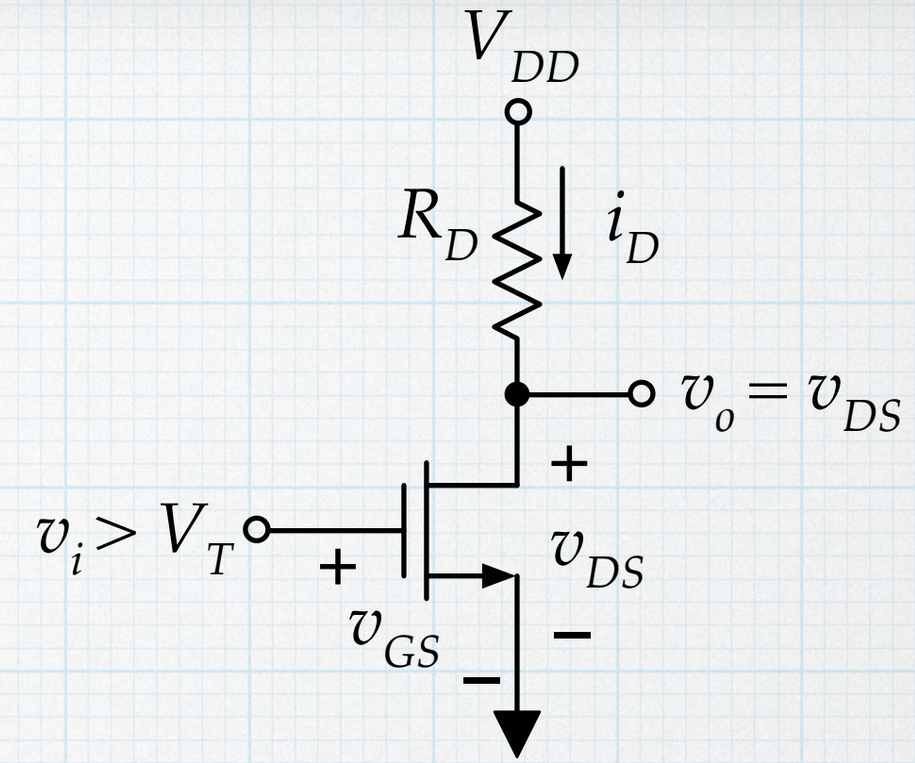


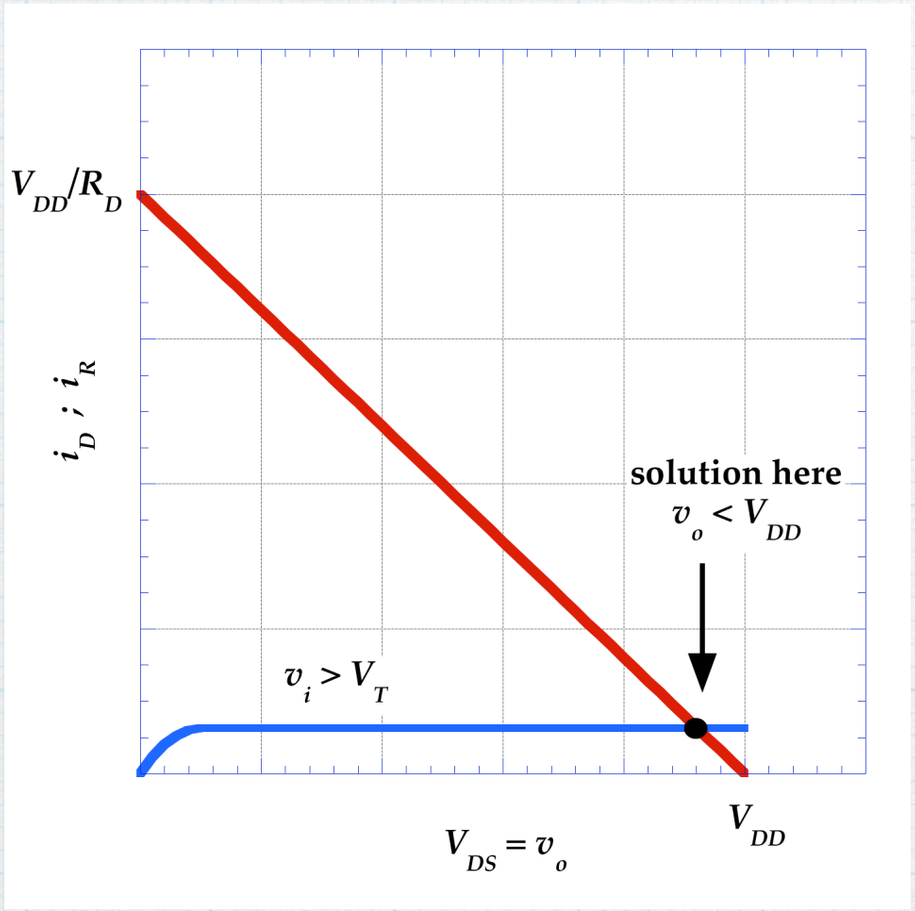




NMOS in saturation

If the input is increased so that $v_i > V_T$ (but not too much bigger), the NMOS will turn on and be operating in the saturation region. A progression of load line diagrams shows what happens as v_i increases.

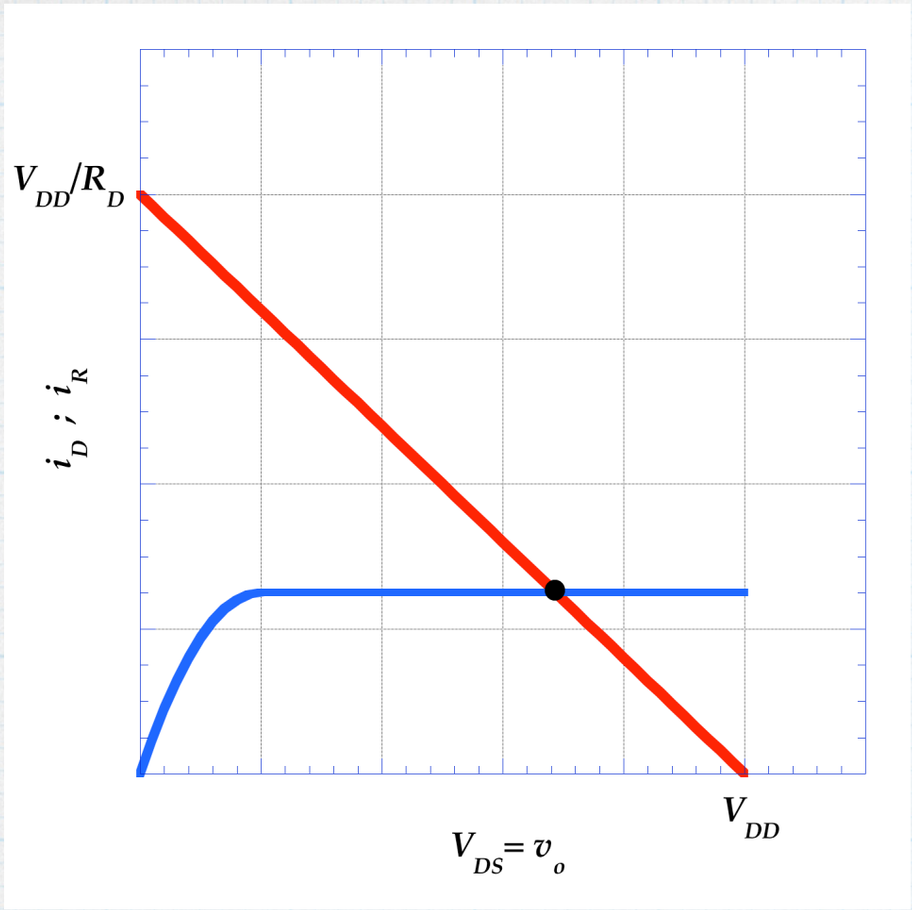


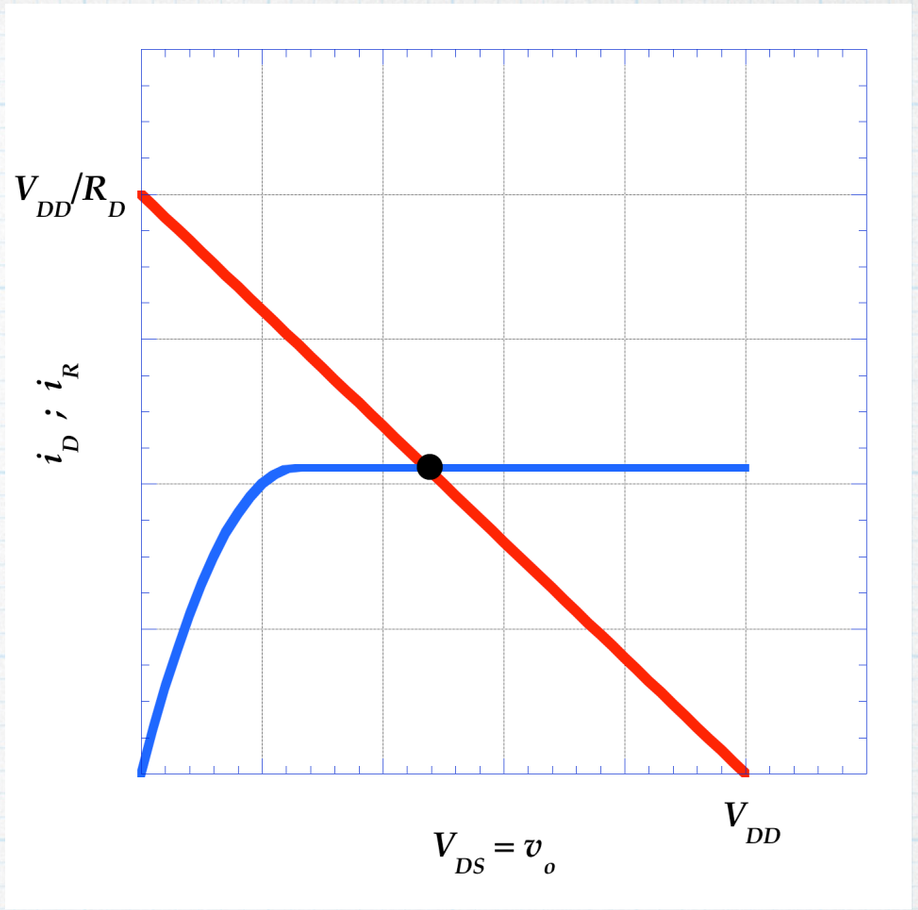


$$i_D = K_n \left(v_i - V_T\right)^2$$

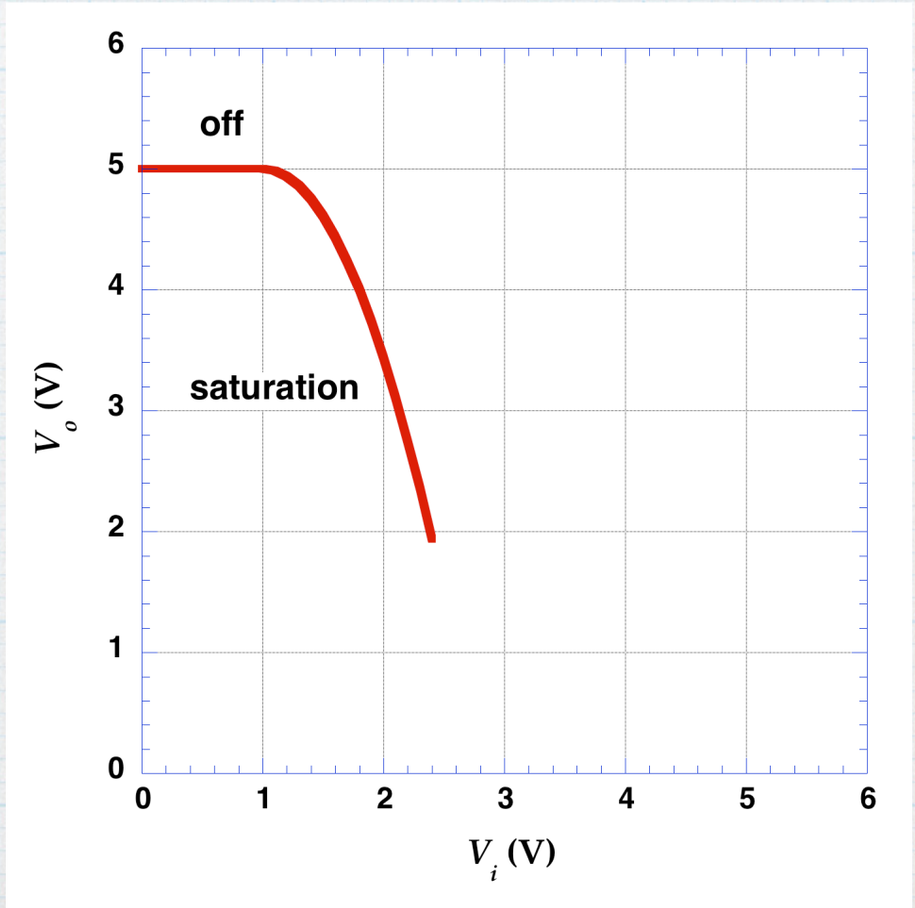
$$v_o = V_{DD} - i_D R_D$$

$$= V_{DD} - K_n R_D \left(v_i - V_T\right)^2$$


V_{DD}/R_D
i_D ; i_R
V_{DD}
$V_{DS} = v_o$

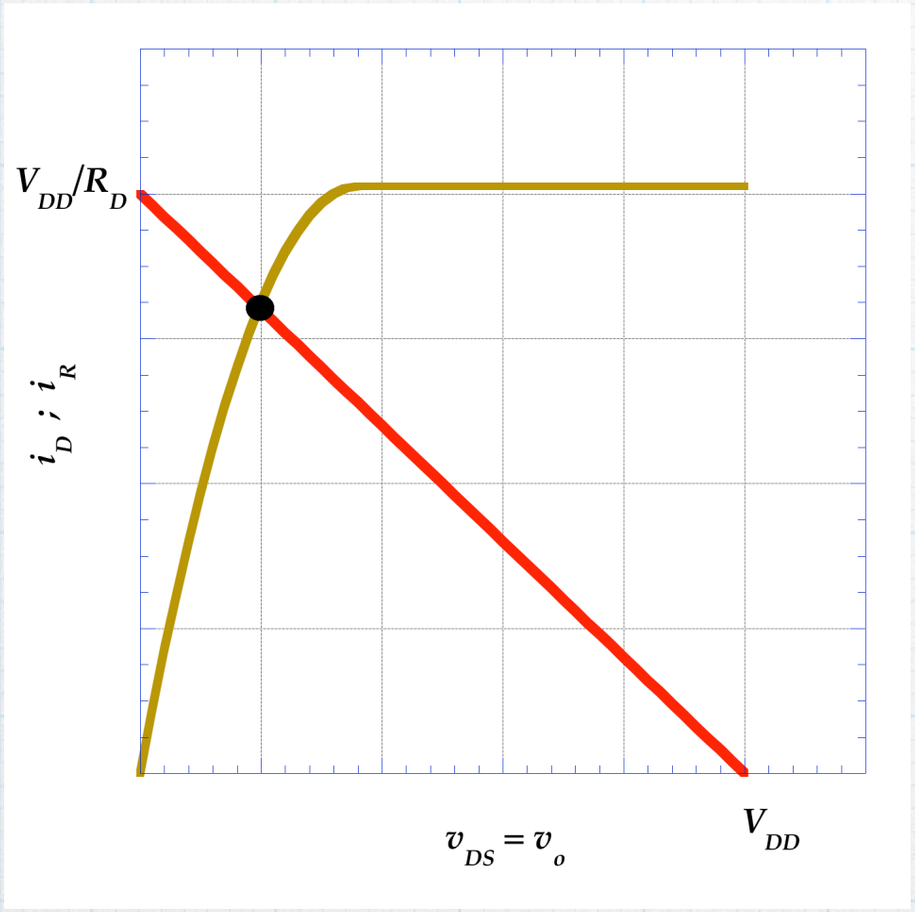

V_{DD}/R_D
i_D ; i_R
V_{DD}
$V_{DS} = v_o$

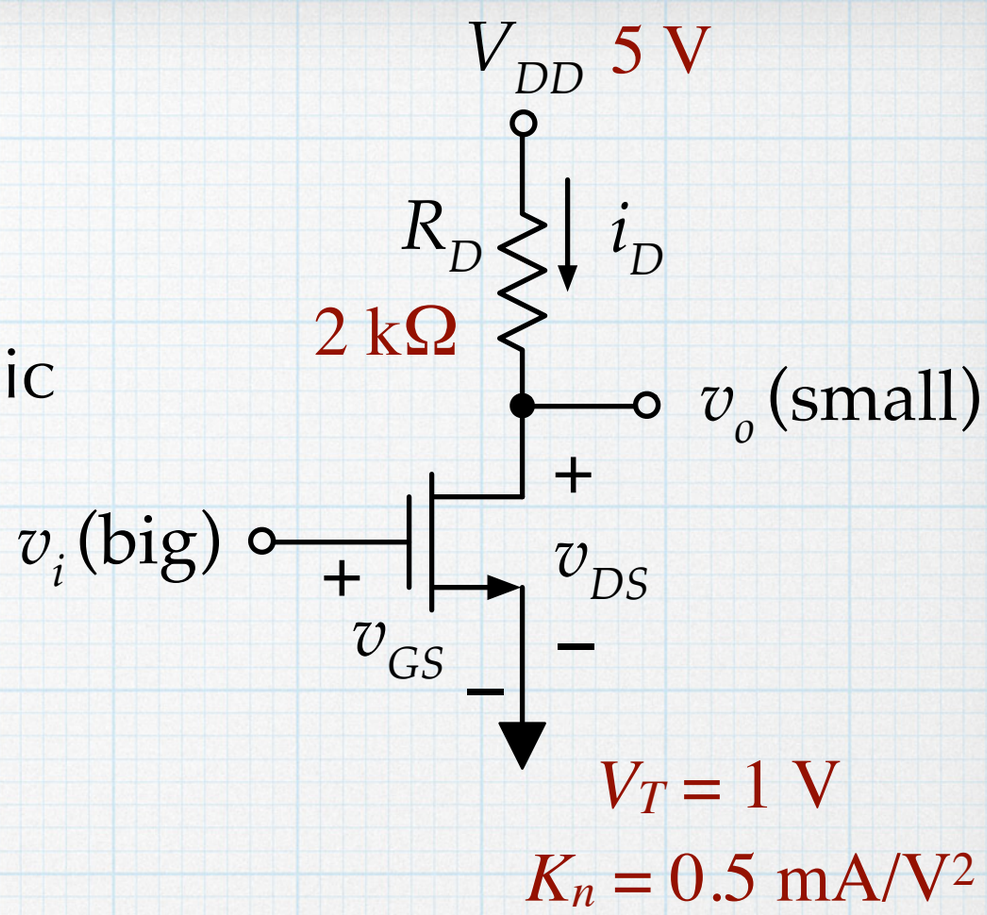
VTC


off
saturation
V_o (V)
V_i (V)
0
1
2
3
4
5
6

NMOS in ohmic

As v_i is increased further, the NMOS curve climbs higher, to the point where the intersection with load line occurs in the ohmic portion of the curve.

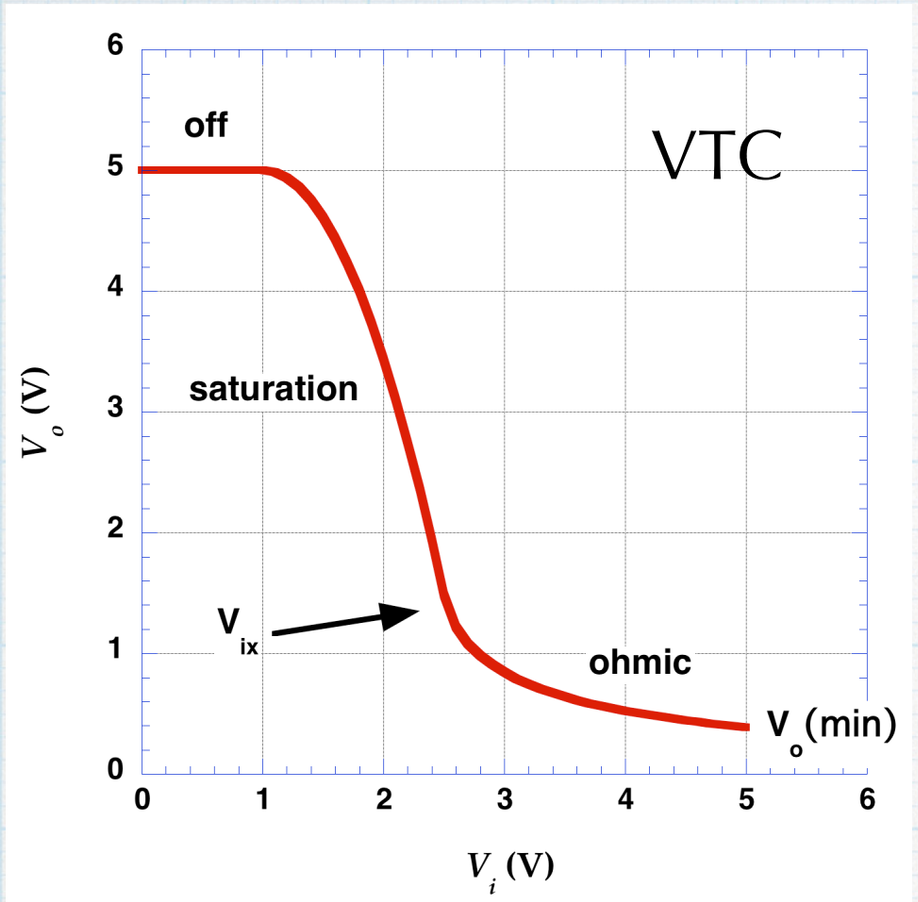




The output goes to the minimum when $v_i = V_{DD}$.

$$\frac{V_{DD} - v_o}{R_D} = K_n \left[2 \left(v_i - V_T \right) v_o - v_o^2 \right]$$ Solve, and take negative root.

$$v_o = \left(v_i - V_T + \frac{1}{2K_n R_D} \right) - \sqrt{\left(v_i - V_T + \frac{1}{2K_n R_D} \right)^2 - \frac{V_{DD}}{K_n R_D}}$$



Boundary between saturation and ohmic: $v_{DS} = v_{GS} - V_T$. Or $v_o = v_i - V_T$. Inserting this relation into either the saturation or ohmic equations, and then solving for V_{ix} gives:

$$V_{ix} = V_T - \frac{1}{2K_nR_D} + \sqrt{\left(\frac{1}{2K_nR_D}\right)^2 + \frac{V_{DD}}{K_nR_D}}$$

(Check it yourself.)

For $v_i < V_T$: $\quad v_o = V_{DD}$

For $V_T < v_i < V_{ix}$: $\quad v_o = V_{DD} - K_nR_D\left(v_i - V_T\right)^2$

For $V_{ix} < v_i < V_{DD}$: $\quad v_o = \left(v_i - V_T + \frac{1}{2K_nR_D}\right) - \sqrt{\left(v_i - V_T + \frac{1}{2K_nR_D}\right)^2 - \frac{V_{DD}}{K_nR_D}}$

Digital operation

To get some sense of how the inverter functions as a logic device, cascade one after the other.

If the input to the first inverter is V_{DD}, it's output will be $v_o(\text{min}) =$. Then the input to the second inverter is , and so it's output will be V_{DD}.

As long as the input is "low enough" the inverter will give an output of V_{DD}. As long the input is "high enough" the inverter will give an output that is "low" (low enough that the next gate will correctly interpret it as logic 0.

This is the power of digital circuitry — voltages don't have to be precise. In this case, "close" is good enough.

Operation as an amplifier

$$v_o = V_{DD} - K_n R_D \left(v_i - V_T\right)^2$$

$$v_i = V_{IDC} + v_{iac}(t) \qquad v_{iac}(t) = V_A \sin \omega t$$

$$v_o = V_{DD} - K_n R_D \left\{ \left[V_{IDC} + v_{iac}(t)\right] - V_T \right\}^2$$

$$= V_{DD} - K_n R_D \left\{ \left[V_{IDC} - V_T\right]^2 + 2\left[V_{IDC} - V_T\right] v_{iac}(t) + \left[v_{iac}(t)\right]^2 \right\}^2$$

$$= \left[V_{DD} - K_n R_D \left(V_{IDC} - V_T\right)^2\right] - \left[2K_n R_D \left(V_{IDC} - V_T\right)\right] v_{iac}(t) - K_n R_D \left[v_{iac}(t)\right]^2$$

$$= V_{ODC} + G_{ac} \cdot v_{iac}(t) - \text{distortion} \qquad G_{ac} - 2K_n R_D \left(V_{IDC} - V_T\right)$$

$$v_o \approx V_{ODC} + G_{ac} \cdot v_{iac}(t)$$